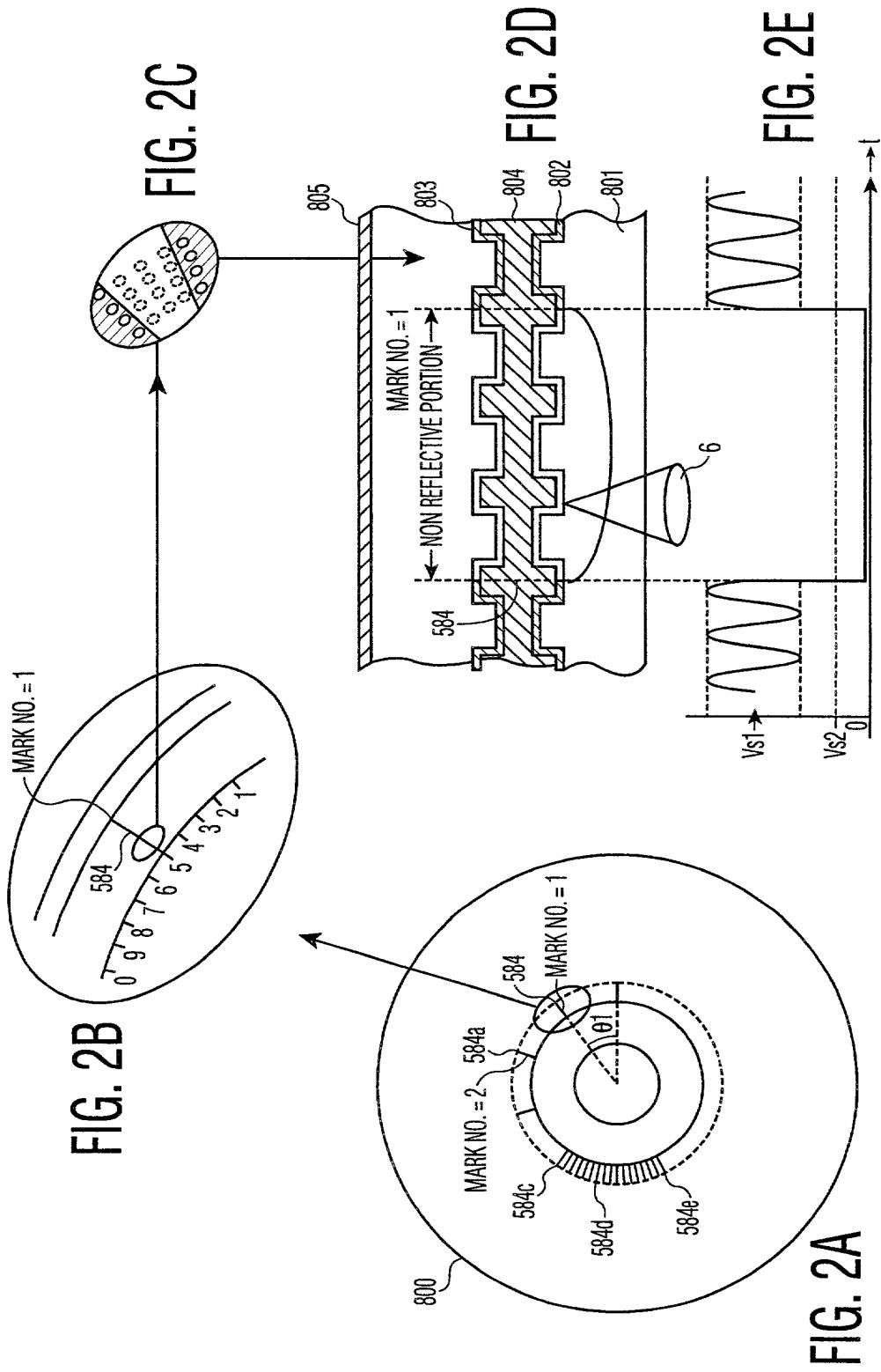


FIG. 1



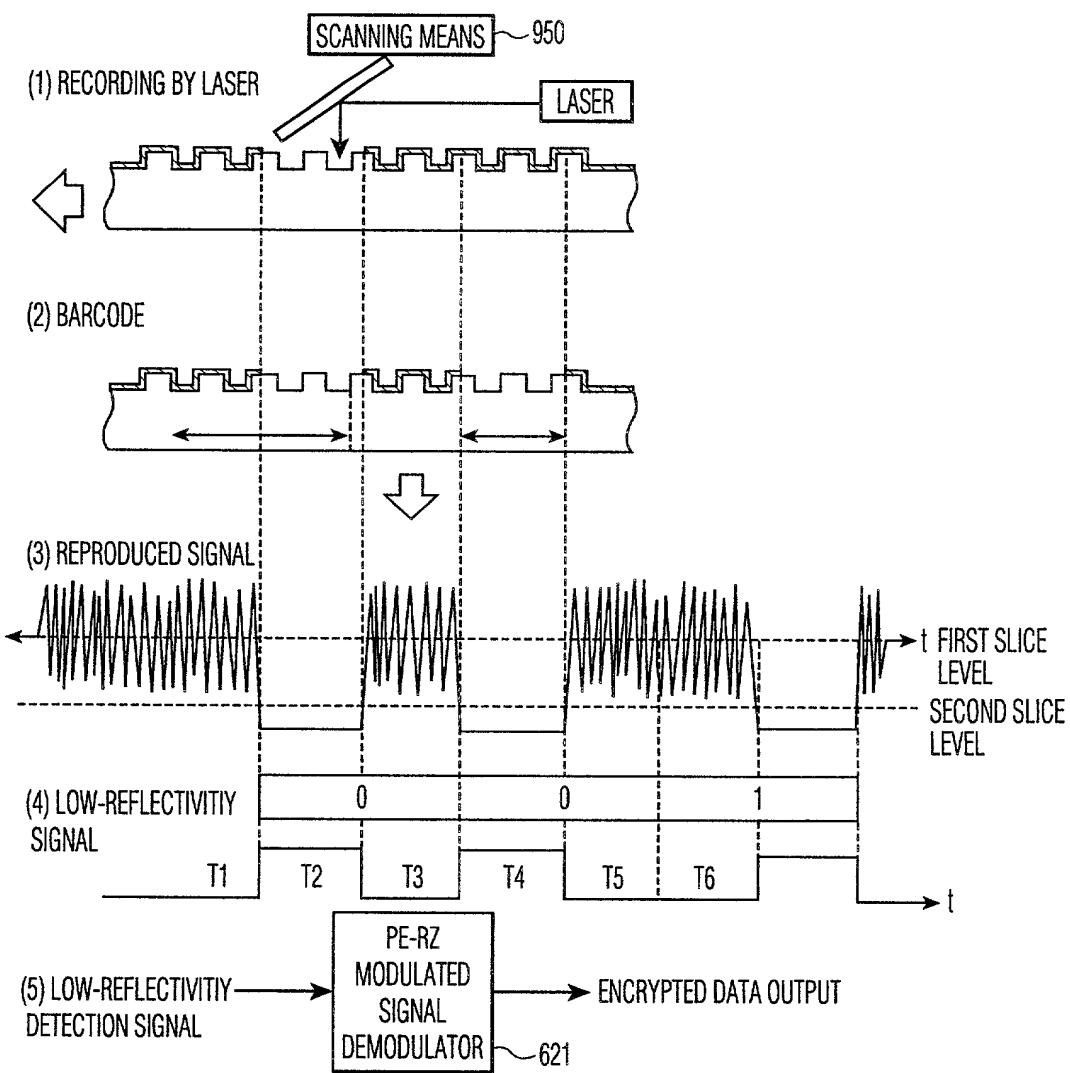


FIG. 3

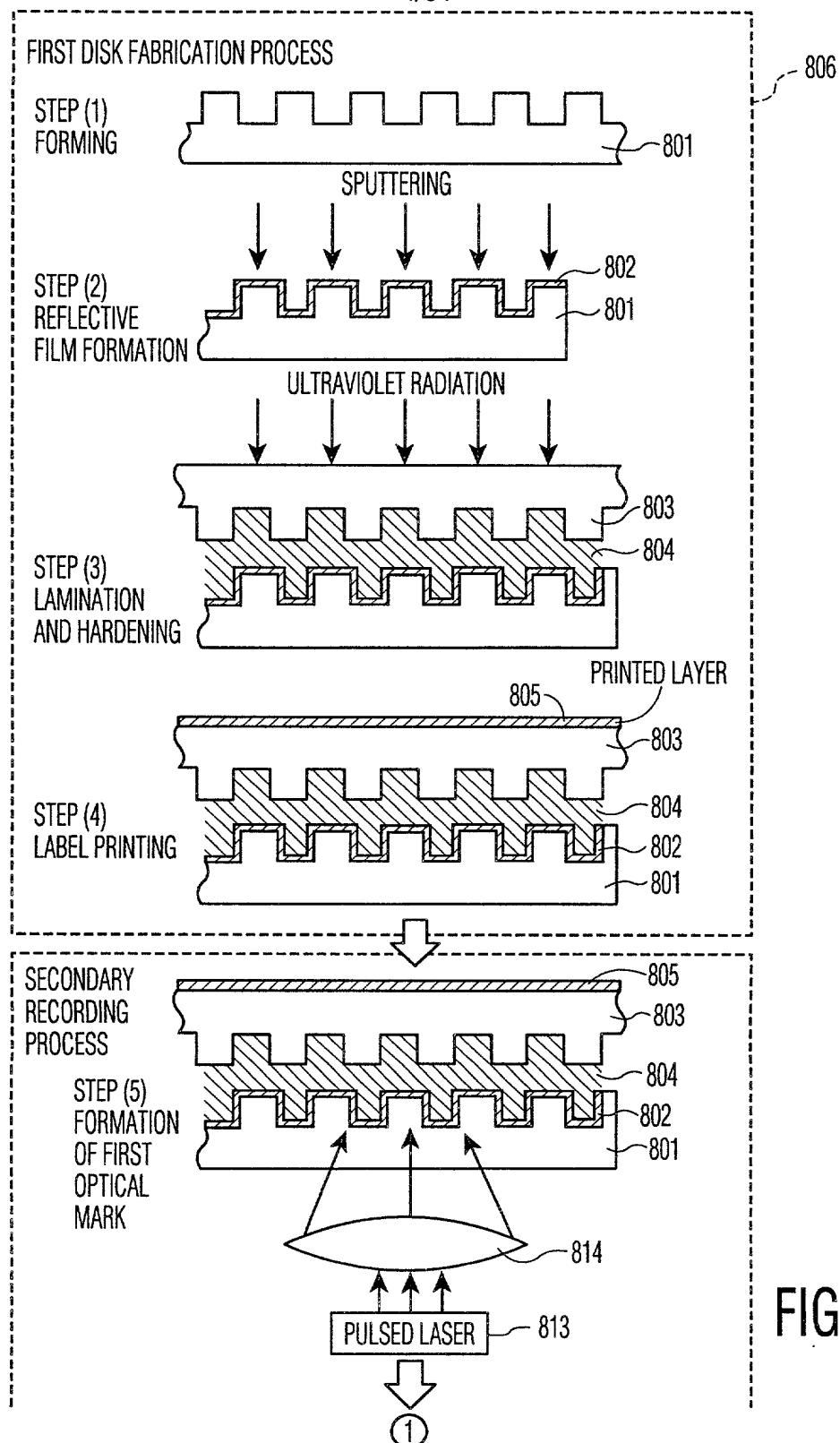
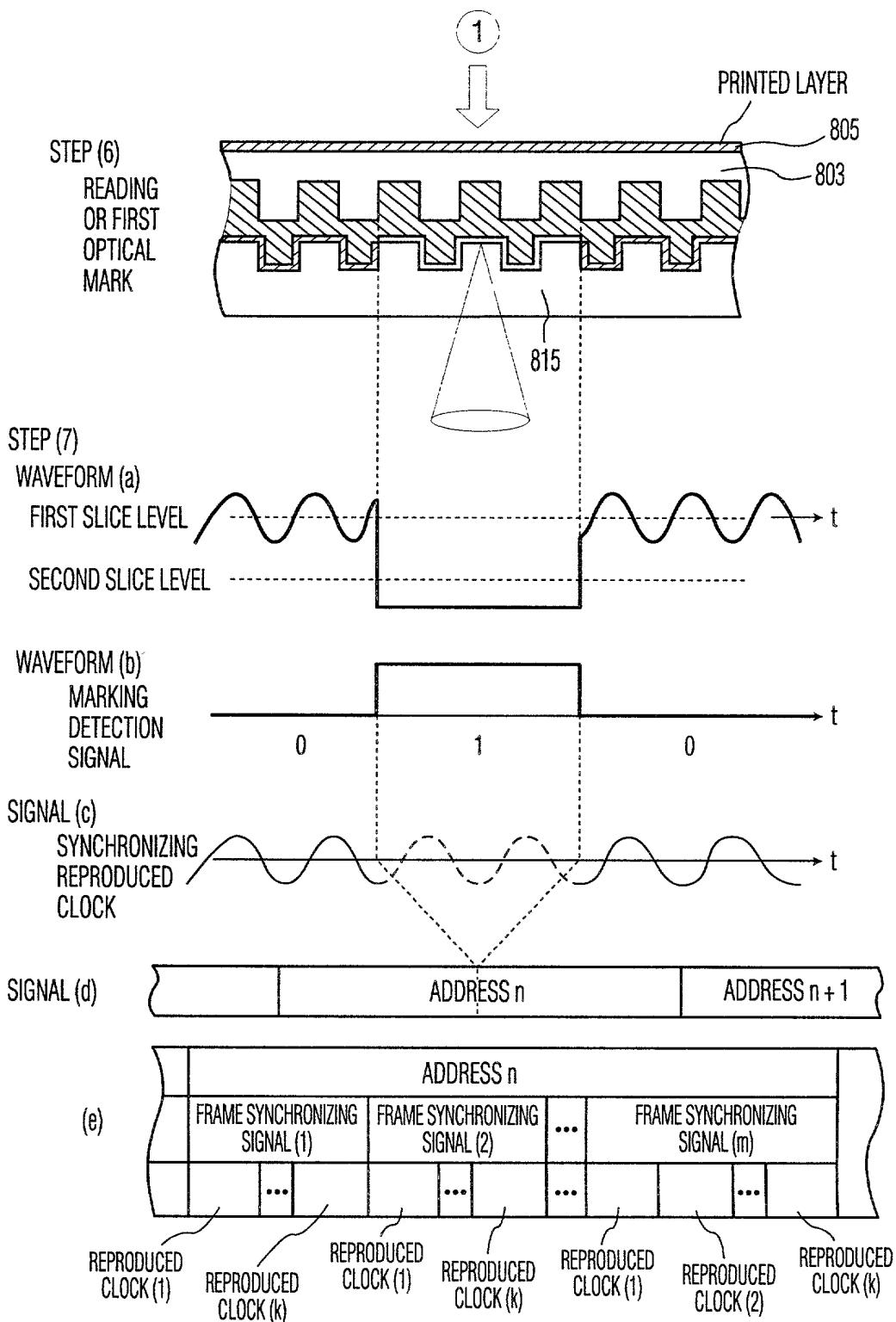


FIG. 4



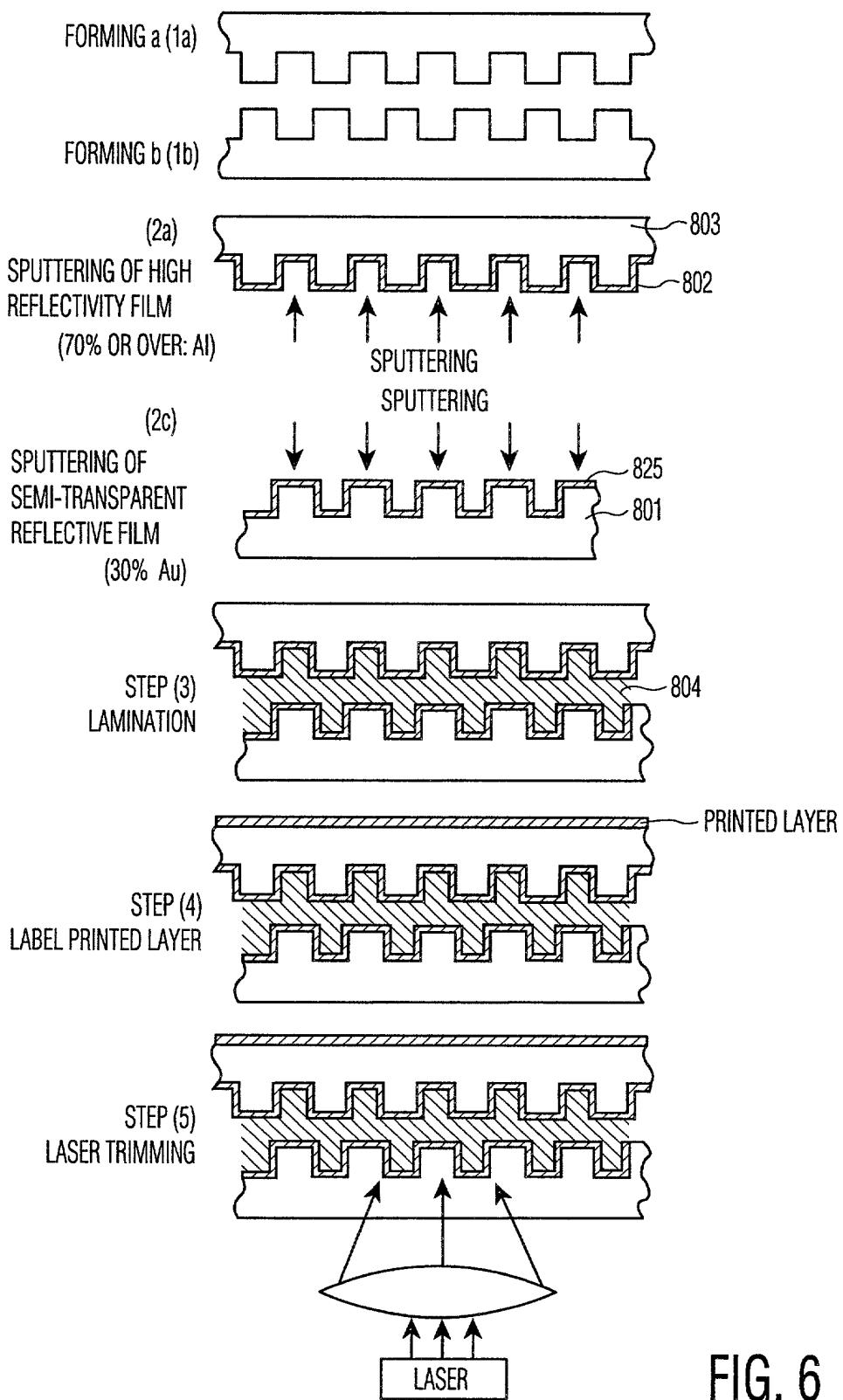


FIG. 6

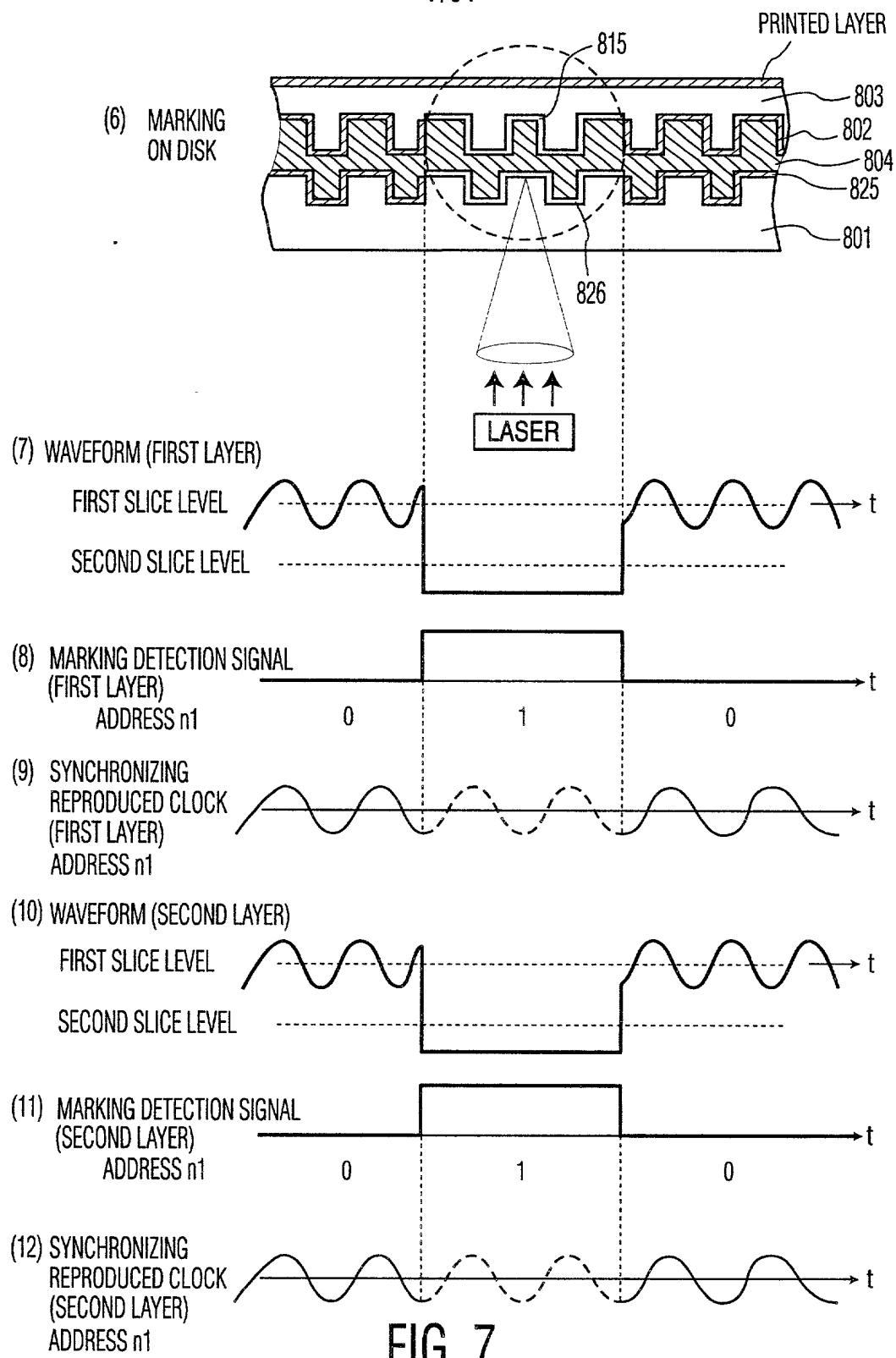


FIG. 7

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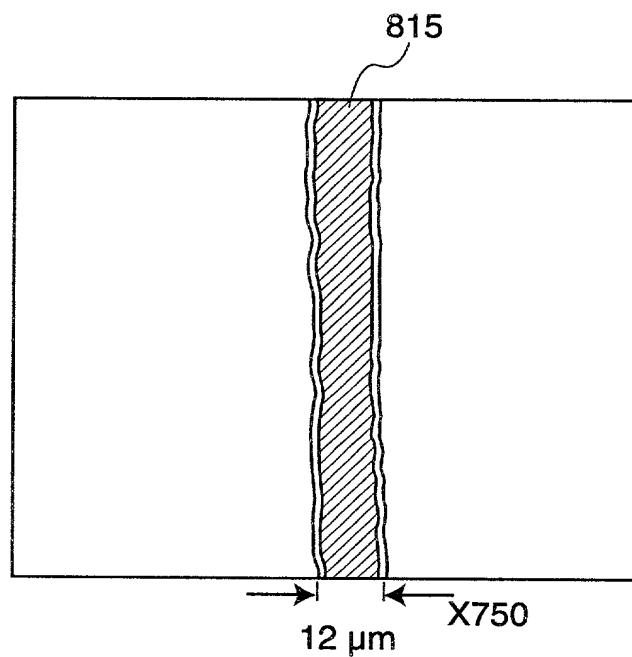


FIG. 8A

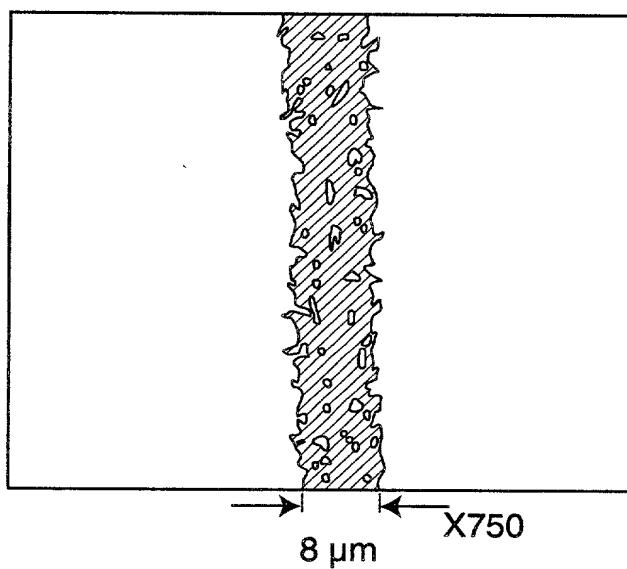


FIG. 8B

FIG. 9A

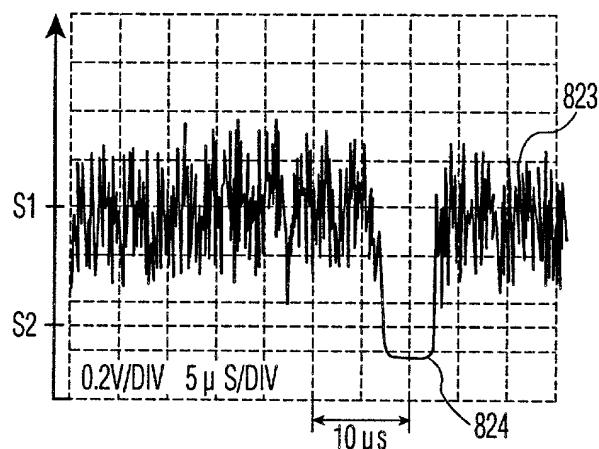


FIG. 9B

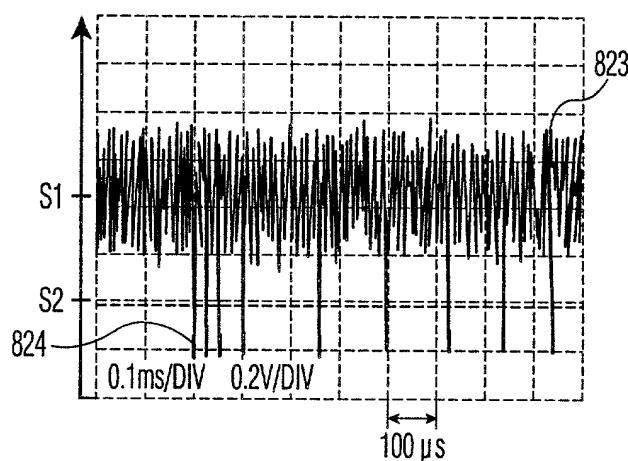


FIG. 9C

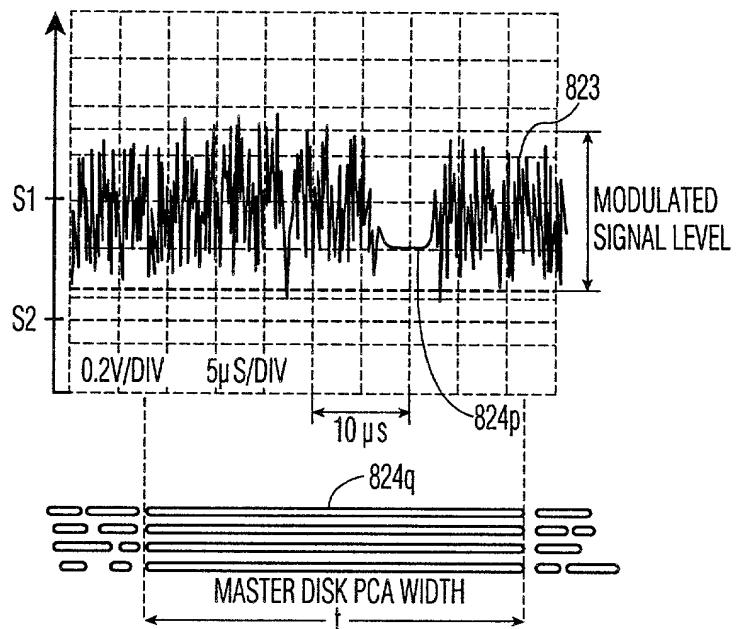
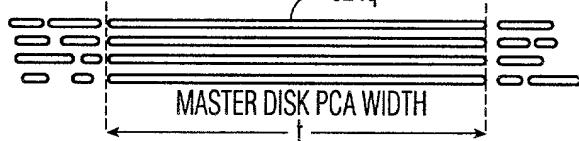
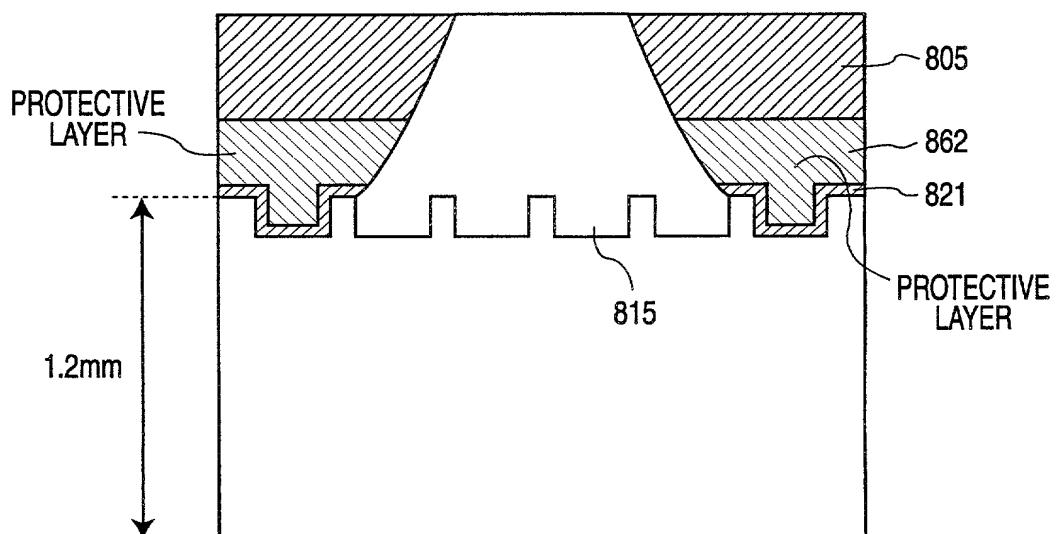
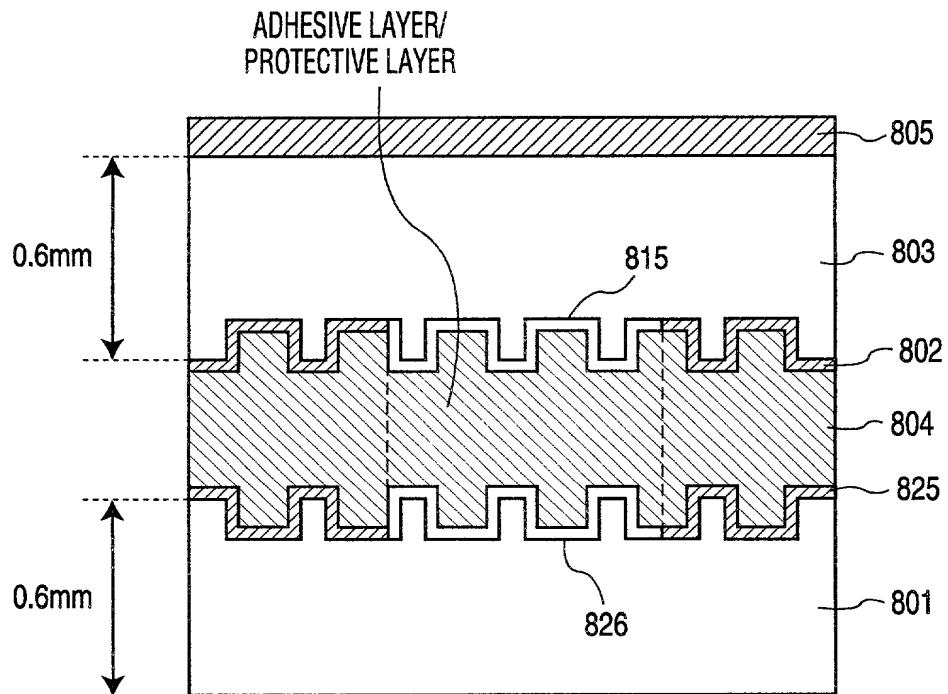


FIG. 9D





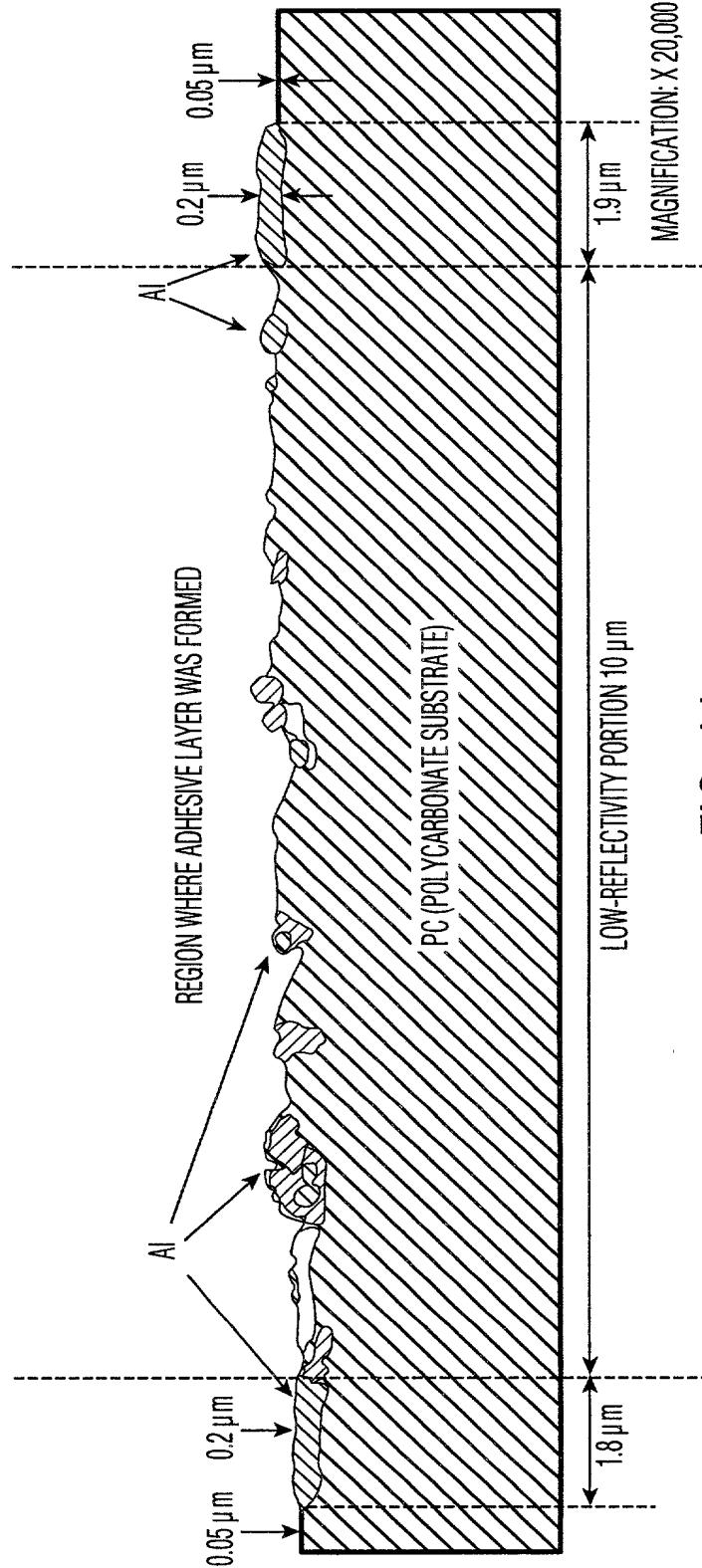


FIG. 11

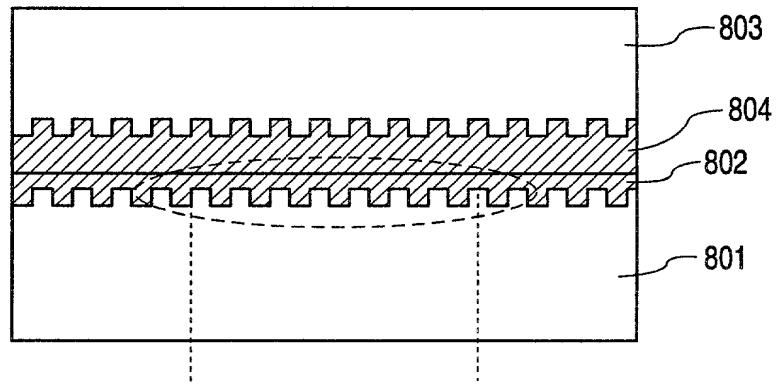


FIG. 12A

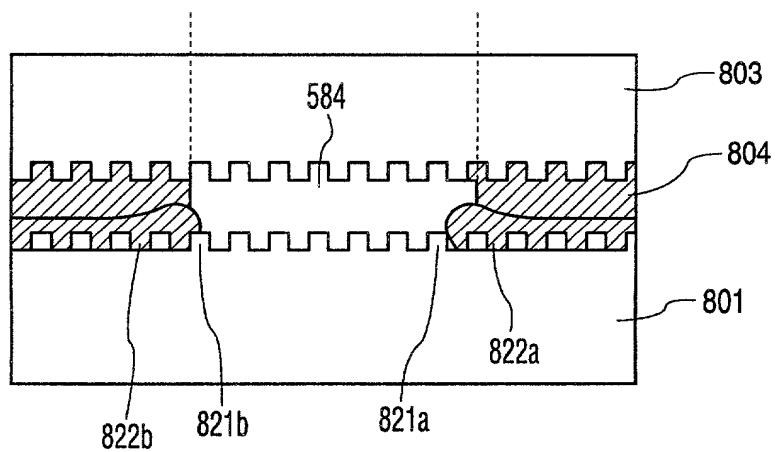


FIG. 12B

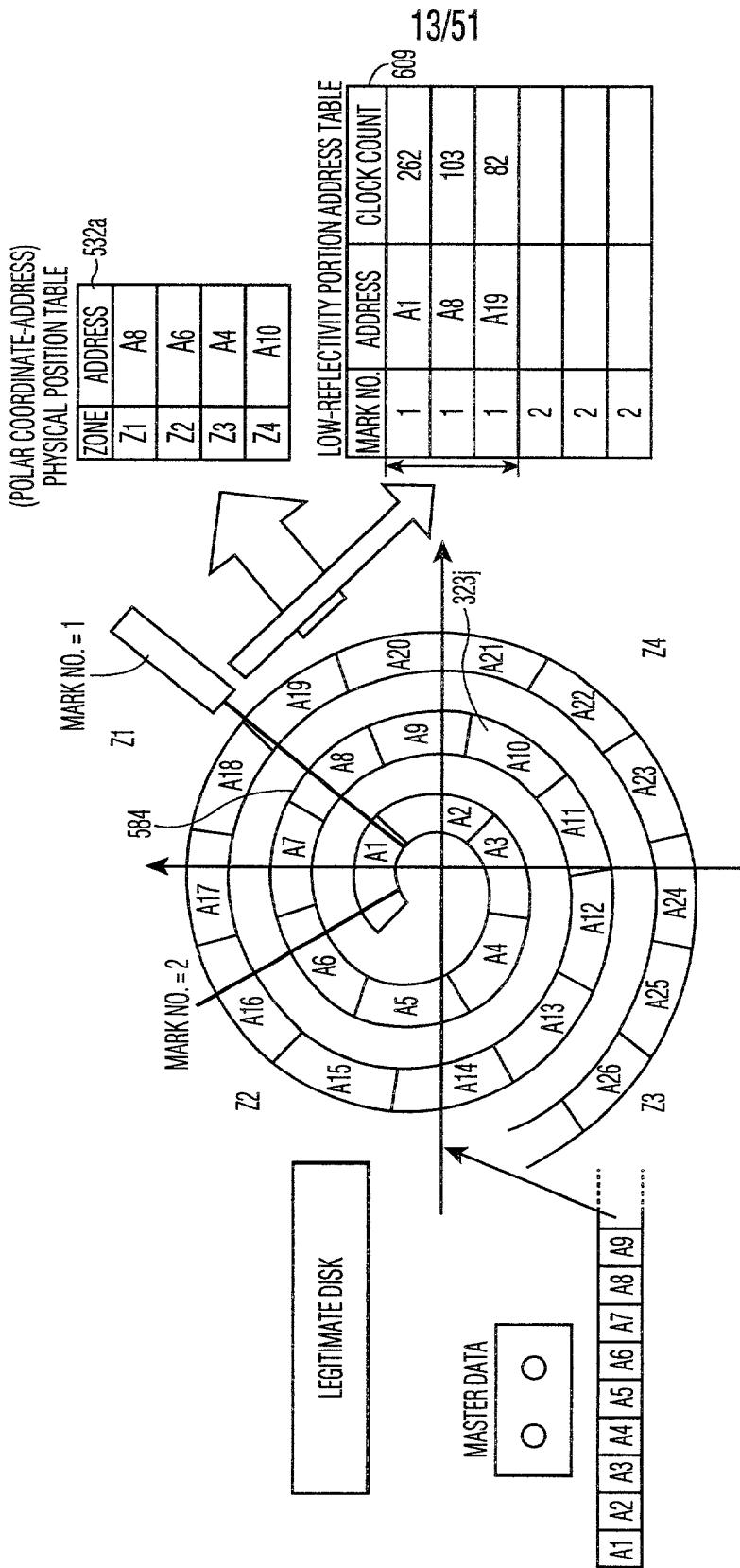


FIG. 13A

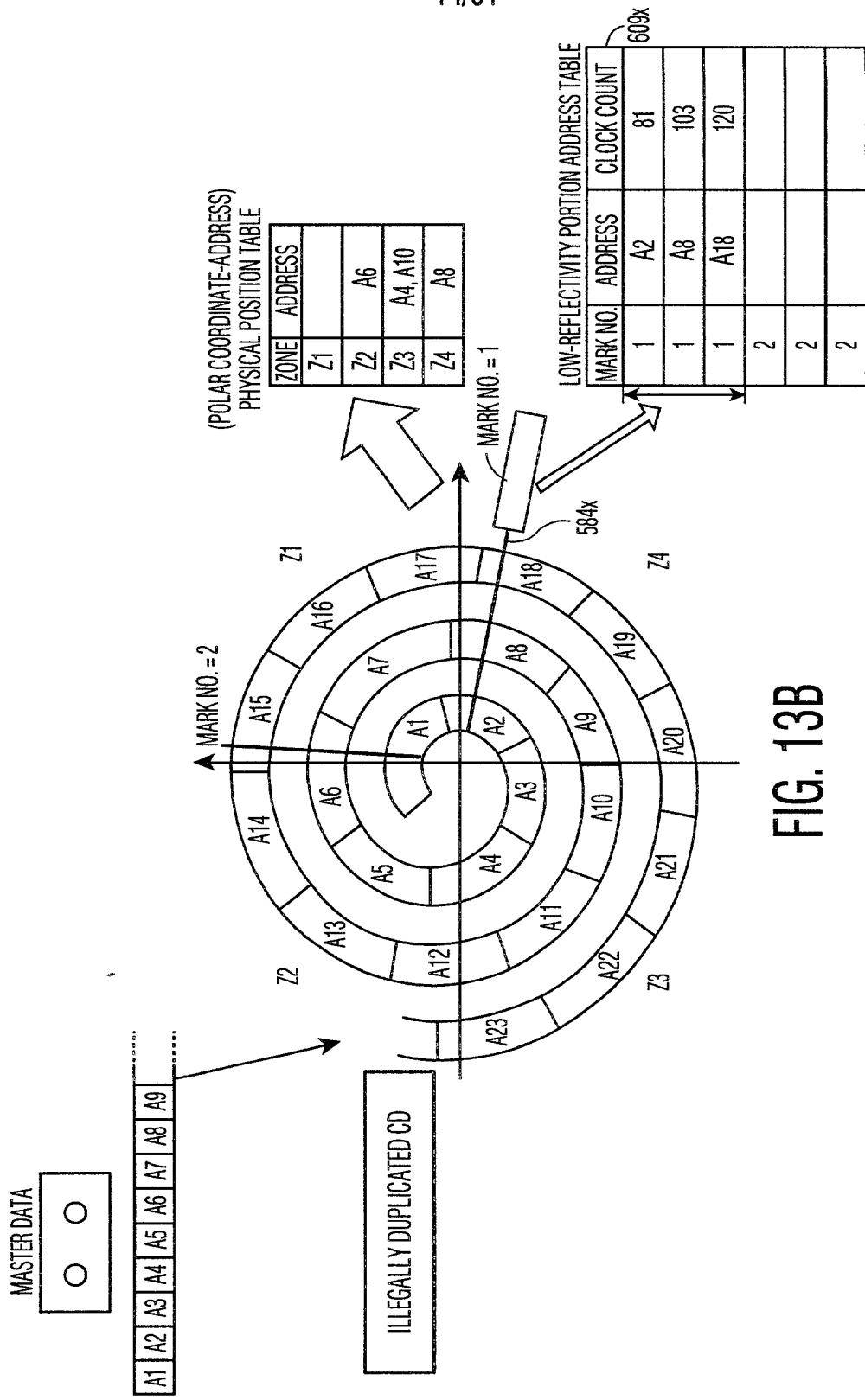


FIG. 13B

FIG. 14A  
FIG. 14B  
FIG. 14C  
FIG. 14D

FIG. 14

**RECORDED DATA  
(WHEN n=1)**

The diagram illustrates a data frame structure with the following components and dimensions:

- 1B:** A vertical column on the left.
- 4B:** A horizontal span across the top.
- 1 ROW:** A vertical span on the right.
- PREAMBLE (All 00h):** A row spanning 4B.
- RS 1:** A row spanning 1B.
- I<sub>0</sub> I<sub>1</sub> I<sub>2</sub> I<sub>3</sub>**: Data elements in the first RS 1 row.
- I<sub>4</sub> I<sub>5</sub> I<sub>6</sub> I<sub>7</sub>**: Data elements in the second RS 1 row.
- I<sub>8</sub> I<sub>9</sub> I<sub>10</sub> I<sub>11</sub>**: Data elements in the third RS 1 row.
- EDC (4B):** A row spanning 4B.
- RS 13:** A row spanning 1B.
- C<sub>0,0</sub> C<sub>3,0</sub>**: ECC elements in the first RS 13 row.
- ECC:** A label for the ECC region.
- C<sub>0,3</sub> C<sub>3,3</sub>**: ECC elements in the second RS 13 row.
- POSTAMBLE (All 55h):** A row spanning 4B.
- RS 14:** A row spanning 1B.
- RS 15:** A row spanning 1B.

Arrows indicate vertical spans of **4n ROWS** for the PREAMBLE, EDC, ECC, and POSTAMBLE sections.

FIG. 14A

## EQUIVALENT DATA DATA FOR ECC ENCODING (WHEN $n=1$ )

FIG. 14B

TYPICAL EQUATION  
FOR EDC COMPUTATION  
EDC (ERROR DETECTION CODE) :

$$\begin{aligned} \text{EDC}_{\text{PCA}}(x) &= \sum_{i=0}^{31} b_i \cdot x^i \\ I_{\text{PCA}}(x) &= \sum_{i=32}^{128n-31} b_i \cdot x^i \end{aligned}$$

FIG. 14C

TYPICAL EQUATION  
FOR EDC COMPUTATION  
ECC (ERROR CORRECTION CODE) :

$$\begin{aligned} R_{\text{PCA}}(x) &= \sum_{i=48}^{51} I_{j+4i} \cdot x^{51-i} \\ I_{\text{PCA}}(x) &= \sum_{i=0}^{4n-2} I_{j+4i} \cdot x^{51-i} + D_j \cdot x^{52-4n}, \end{aligned}$$

FIG. 14D

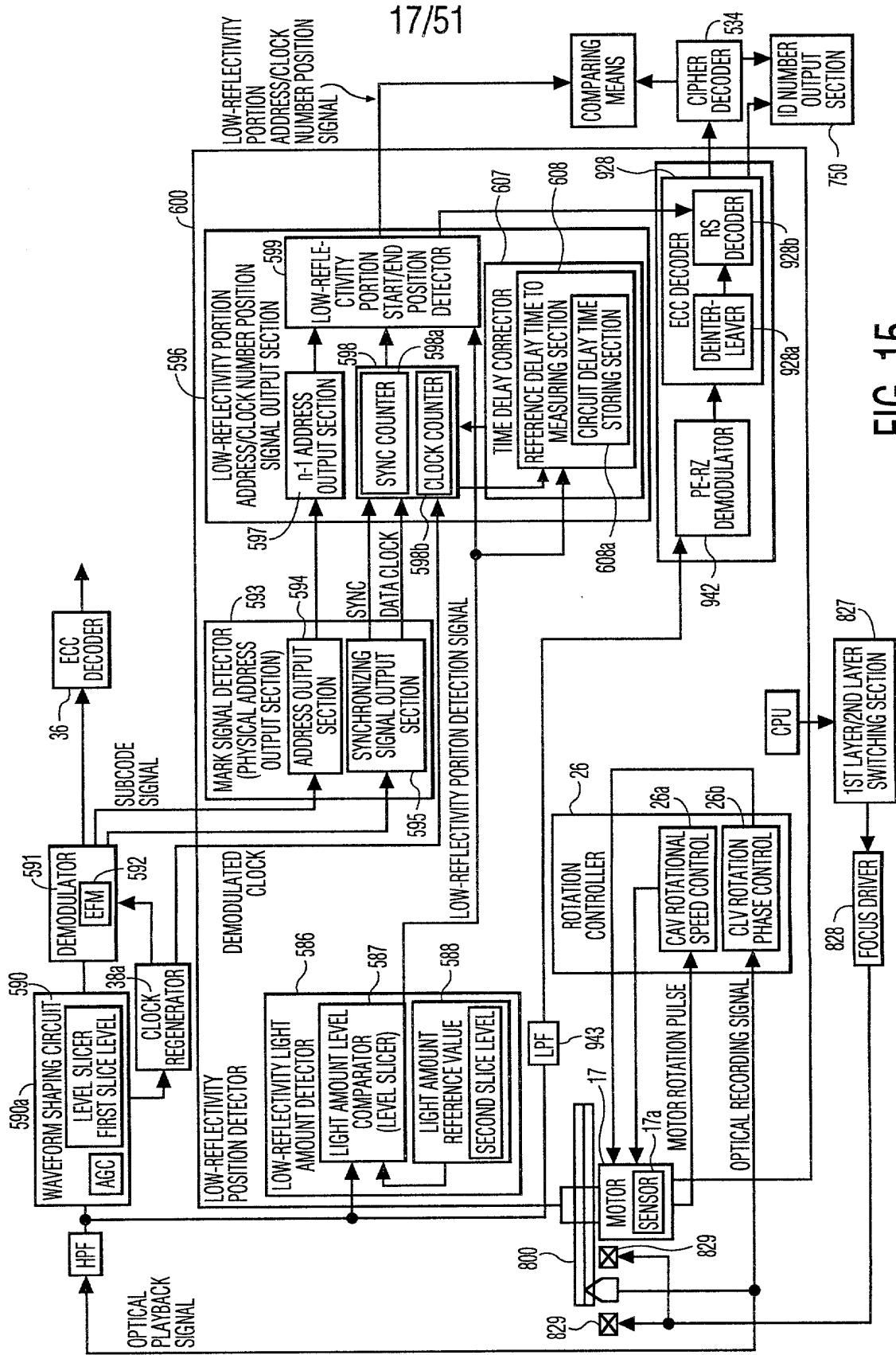


FIG. 15

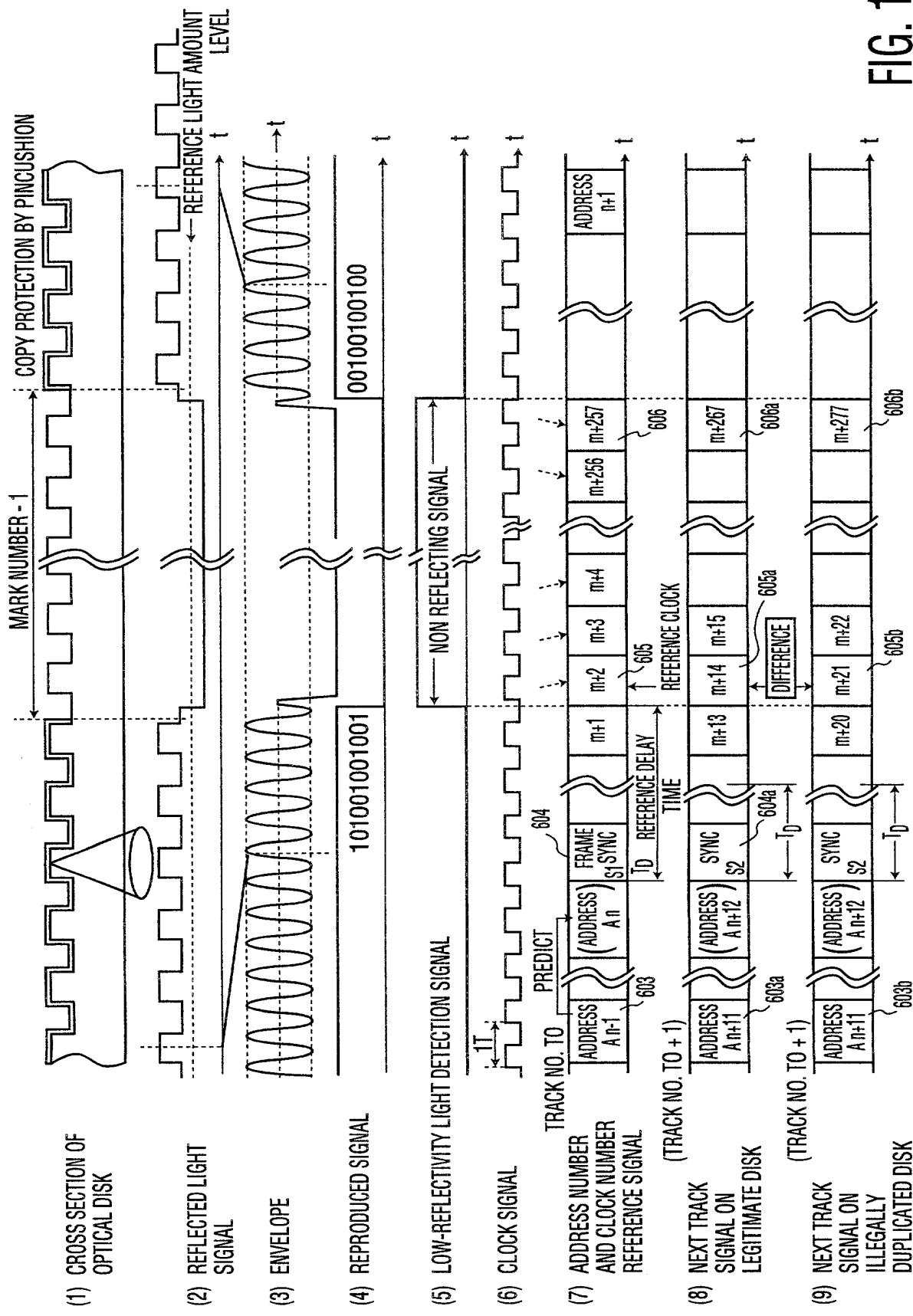


FIG. 16

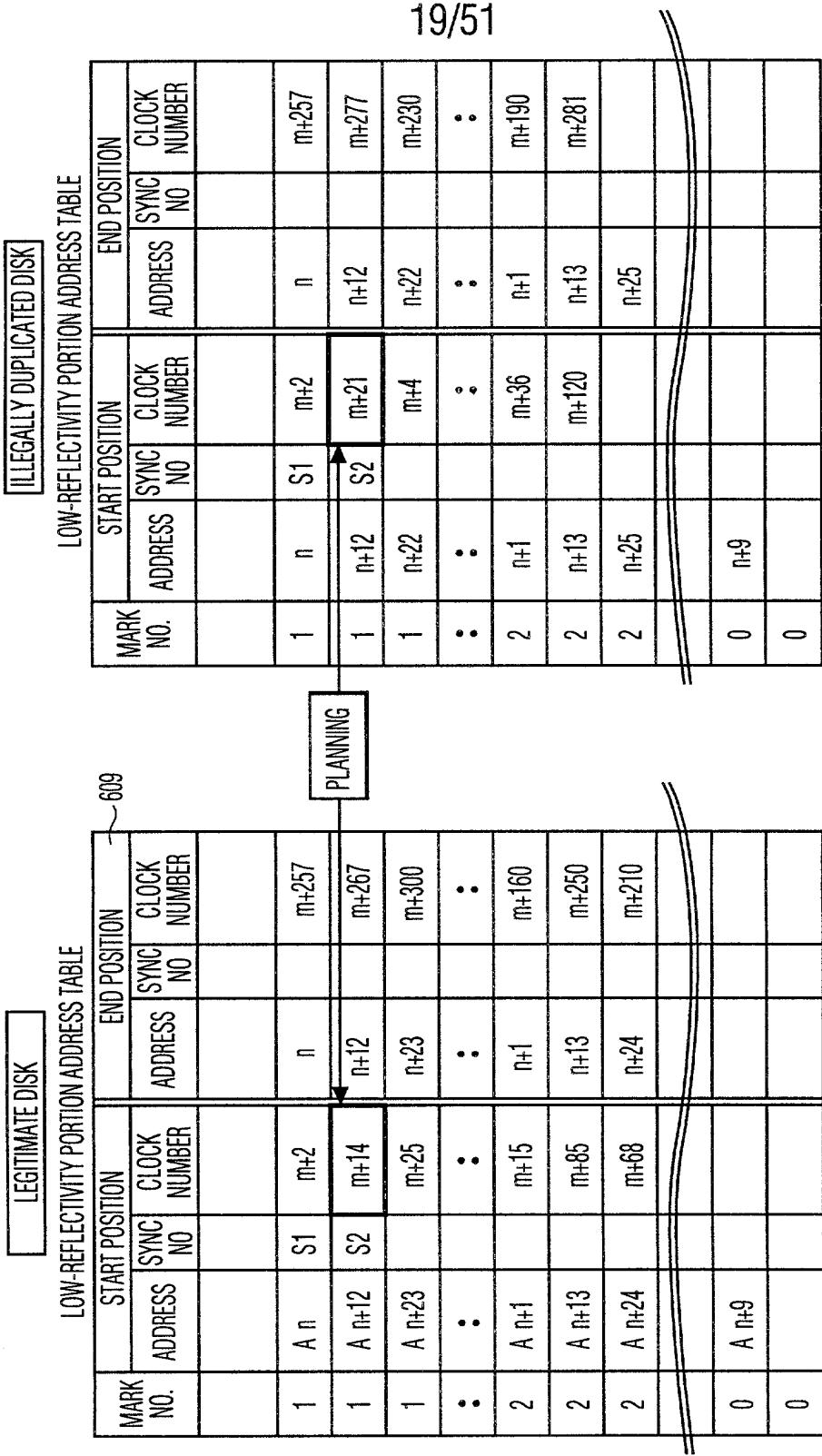


FIG. 17

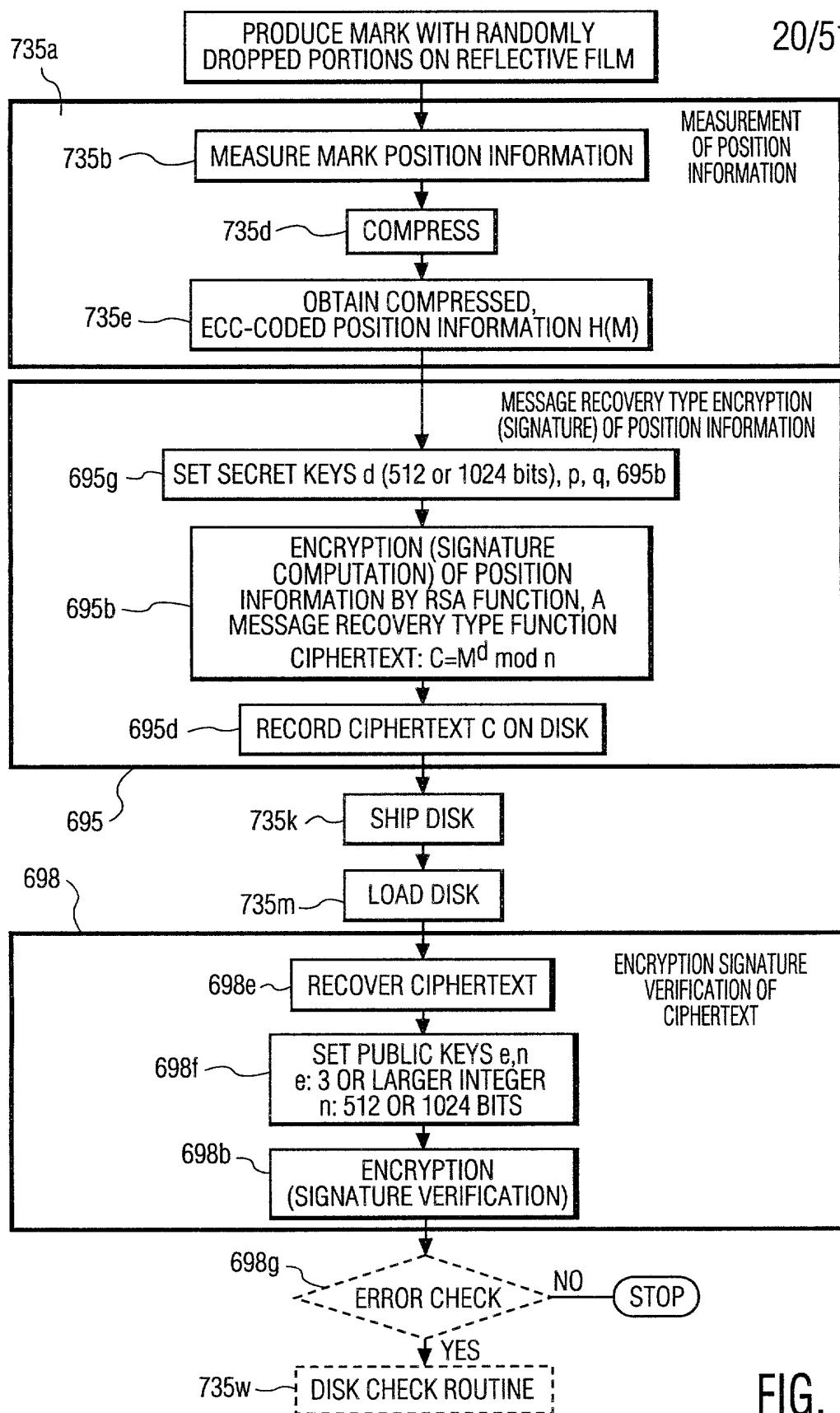


FIG. 18A

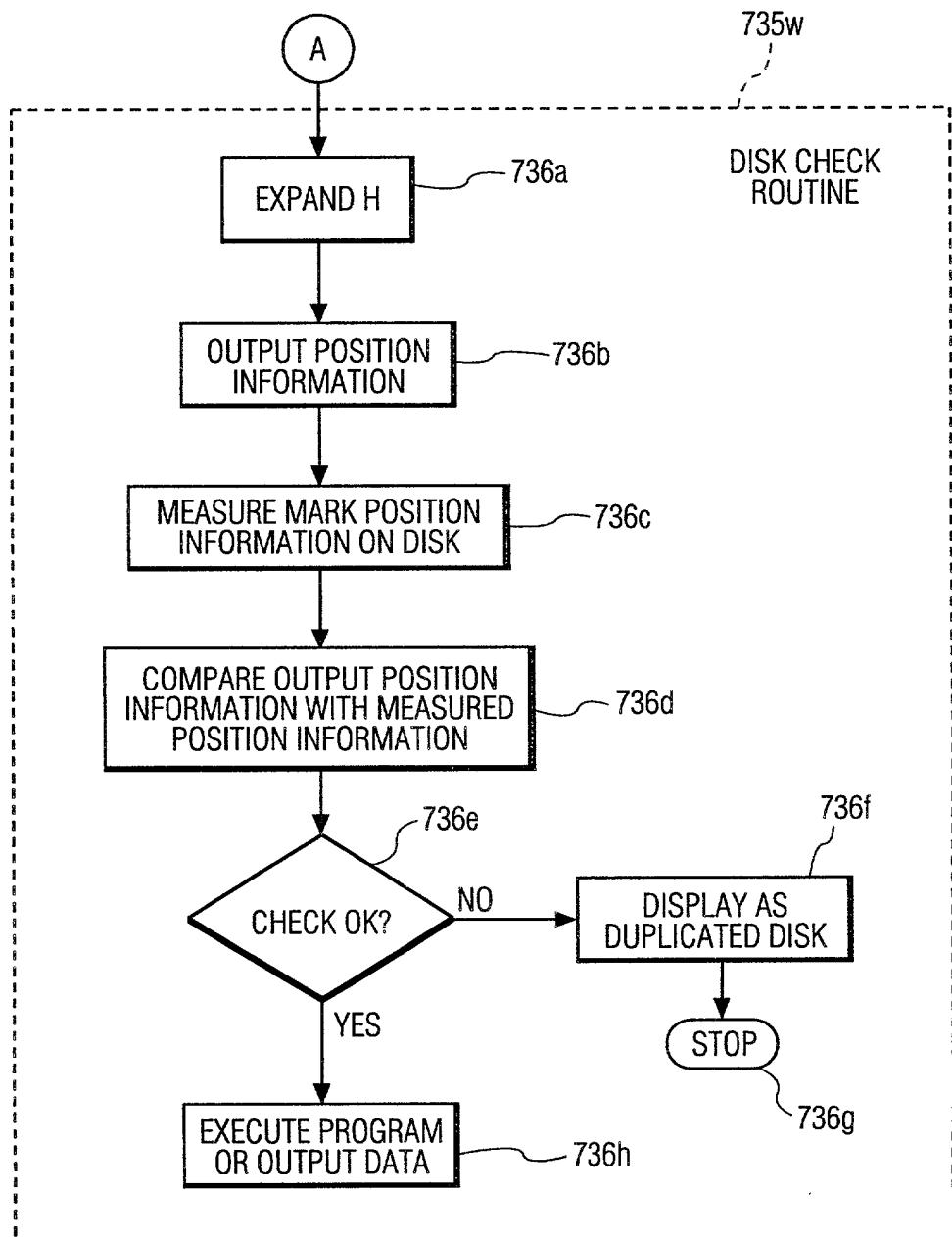


FIG. 18B

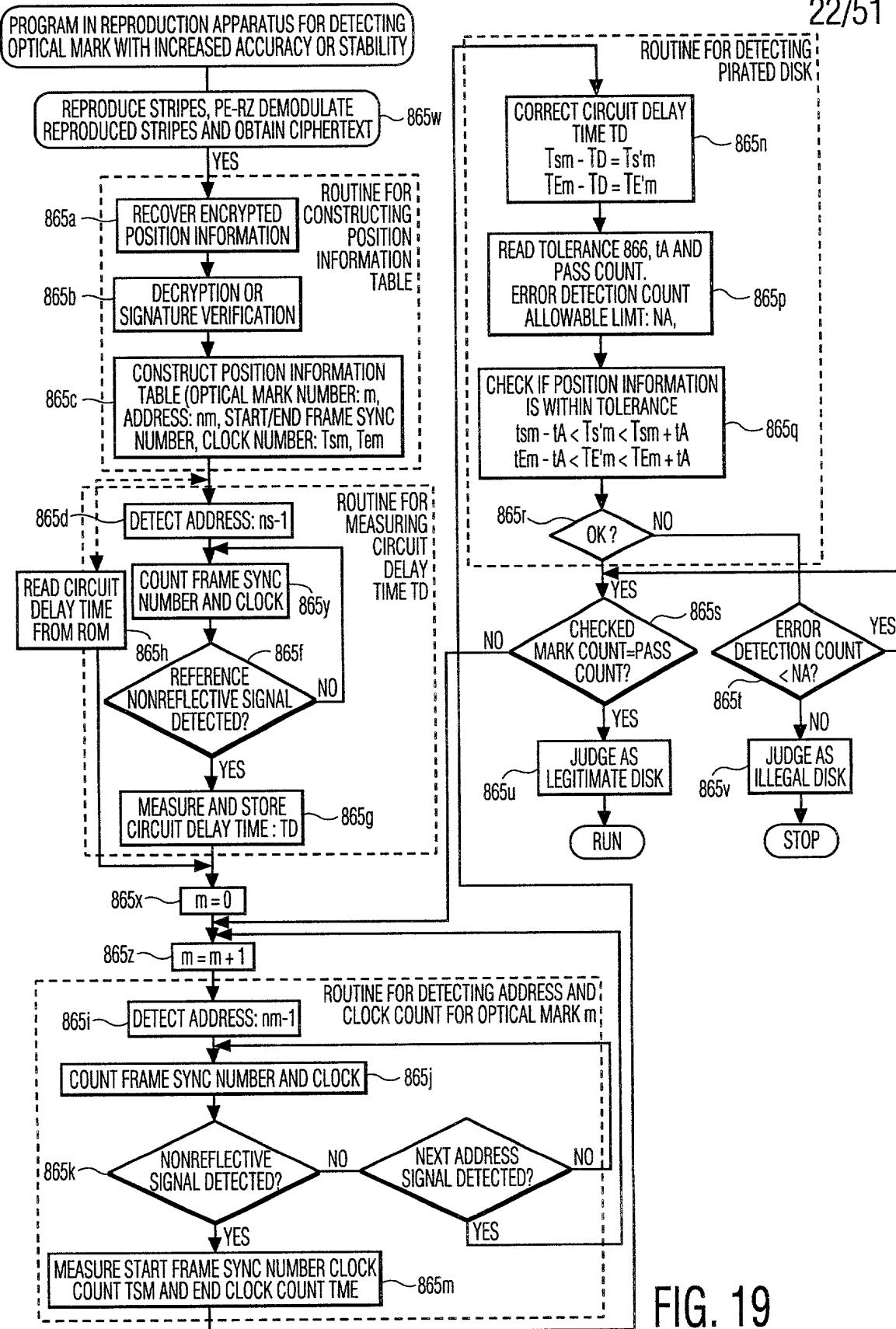


FIG. 19

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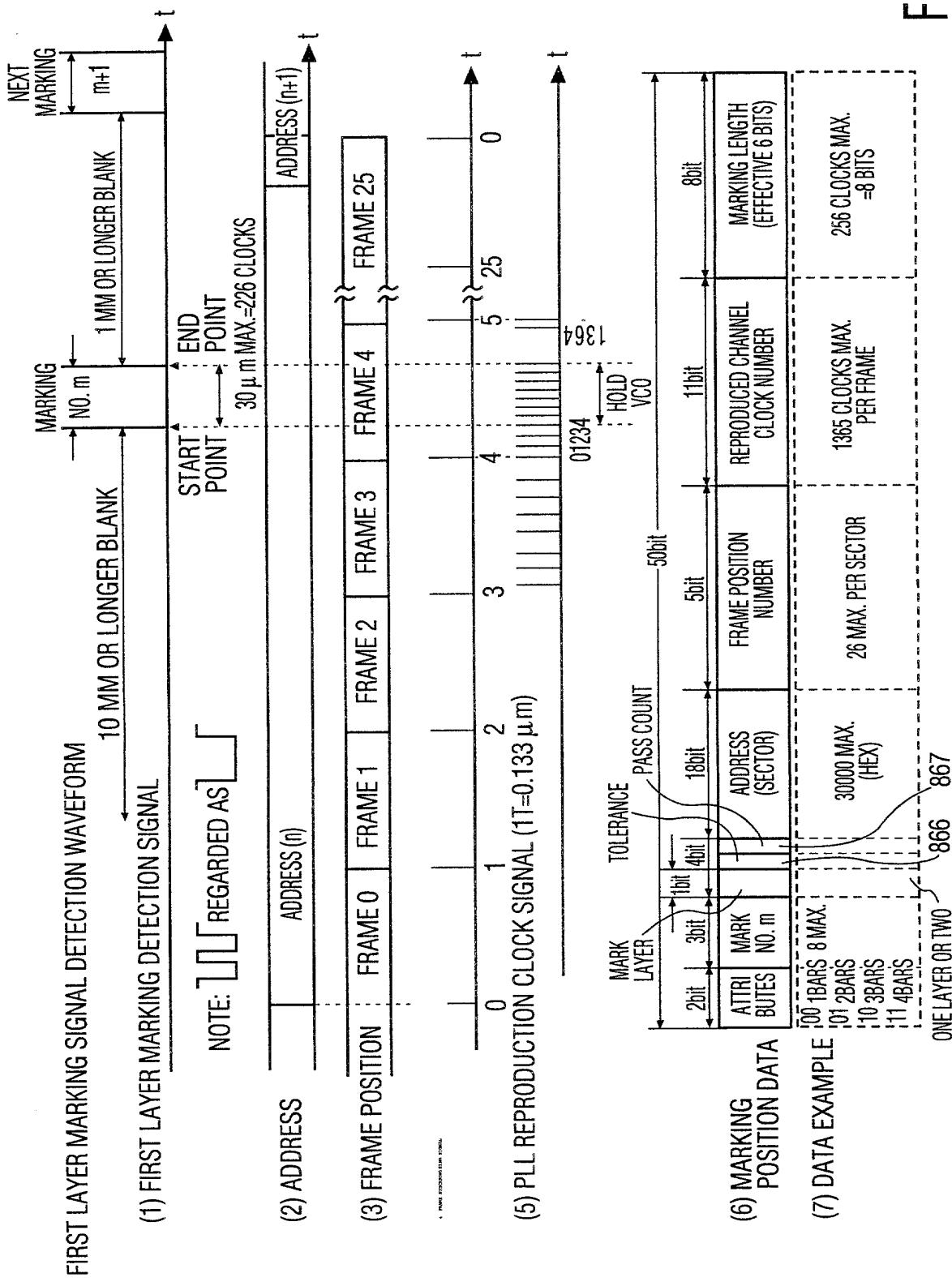
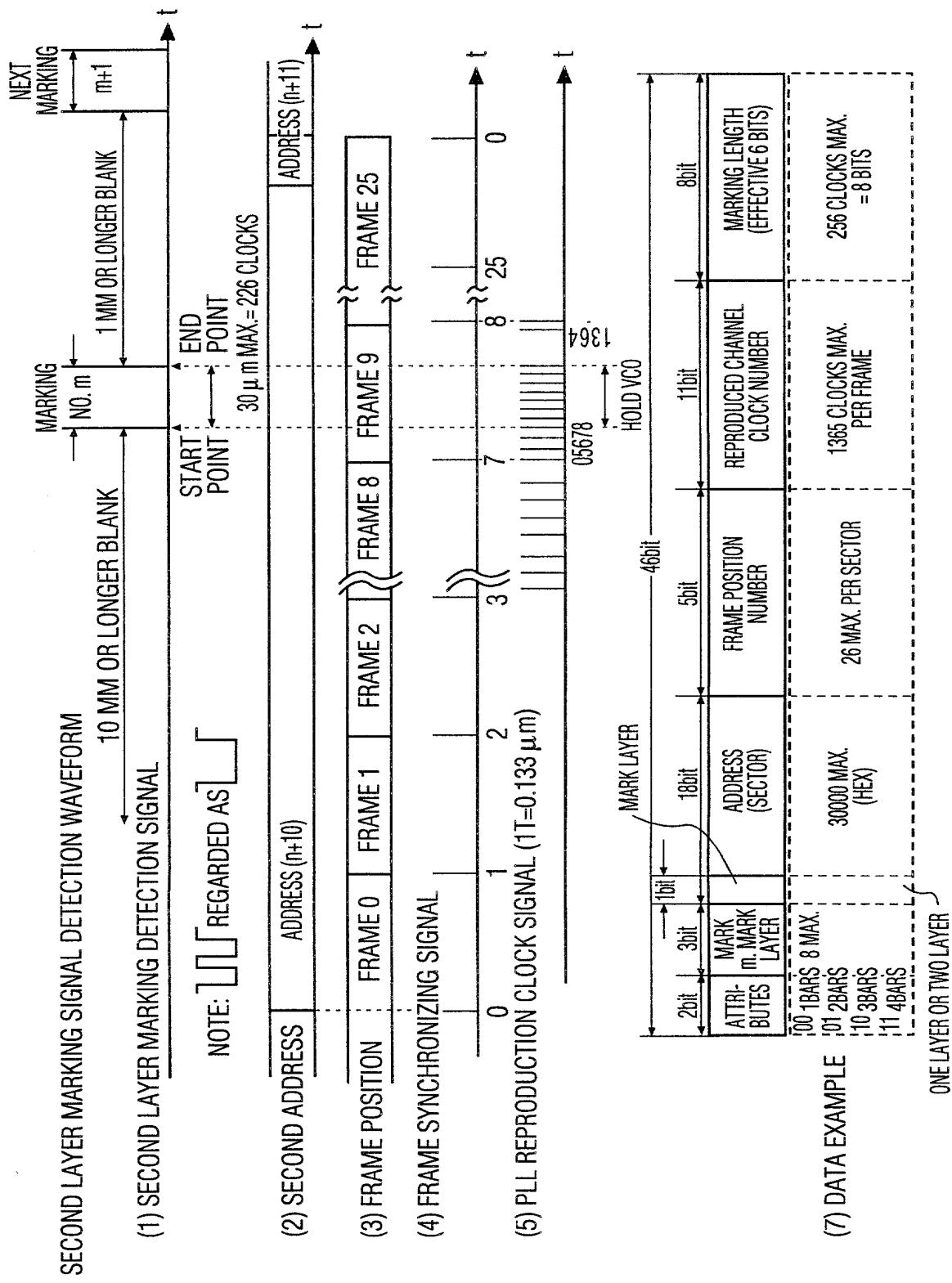


FIG. 20



INSTALLATION START

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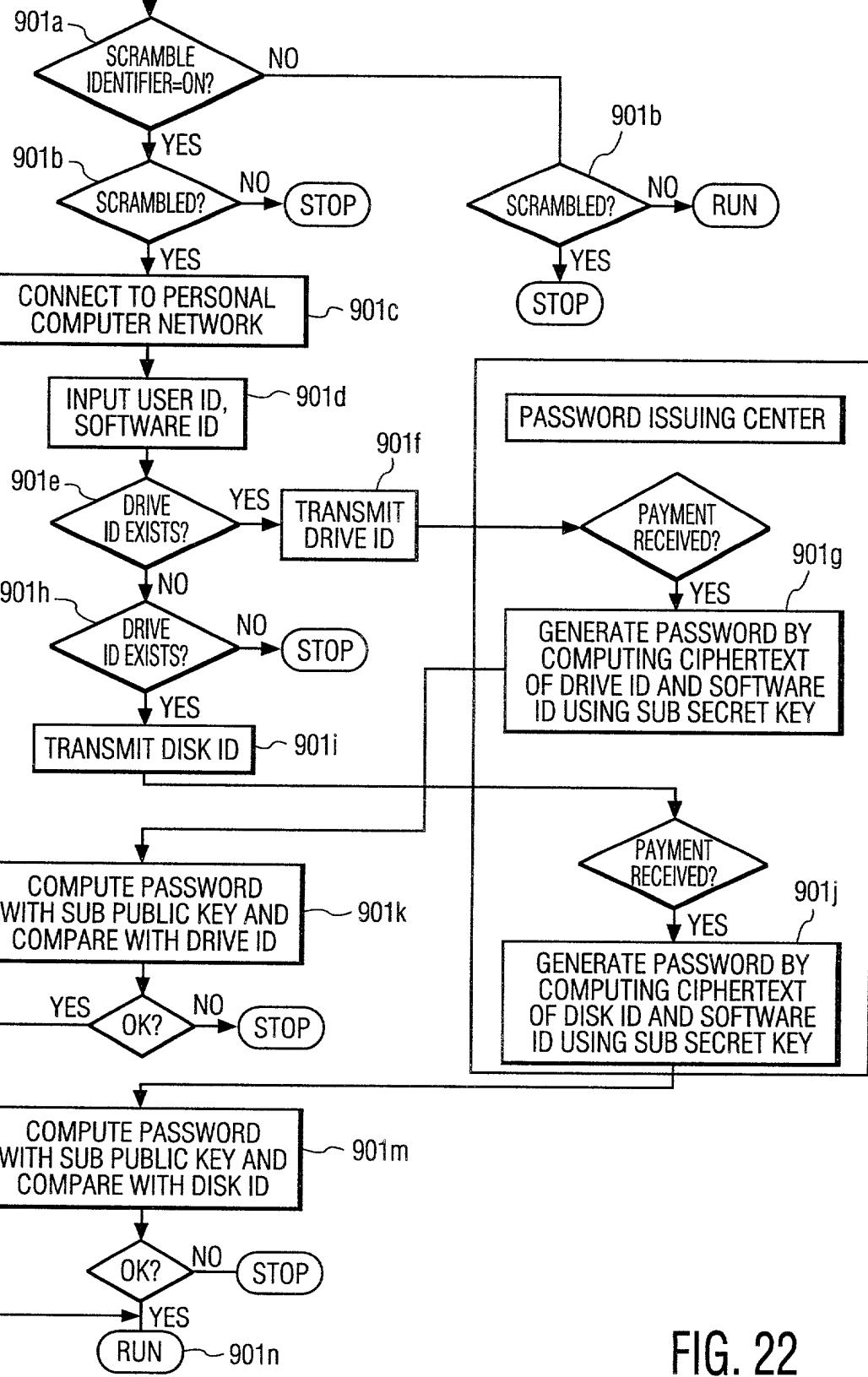


FIG. 22

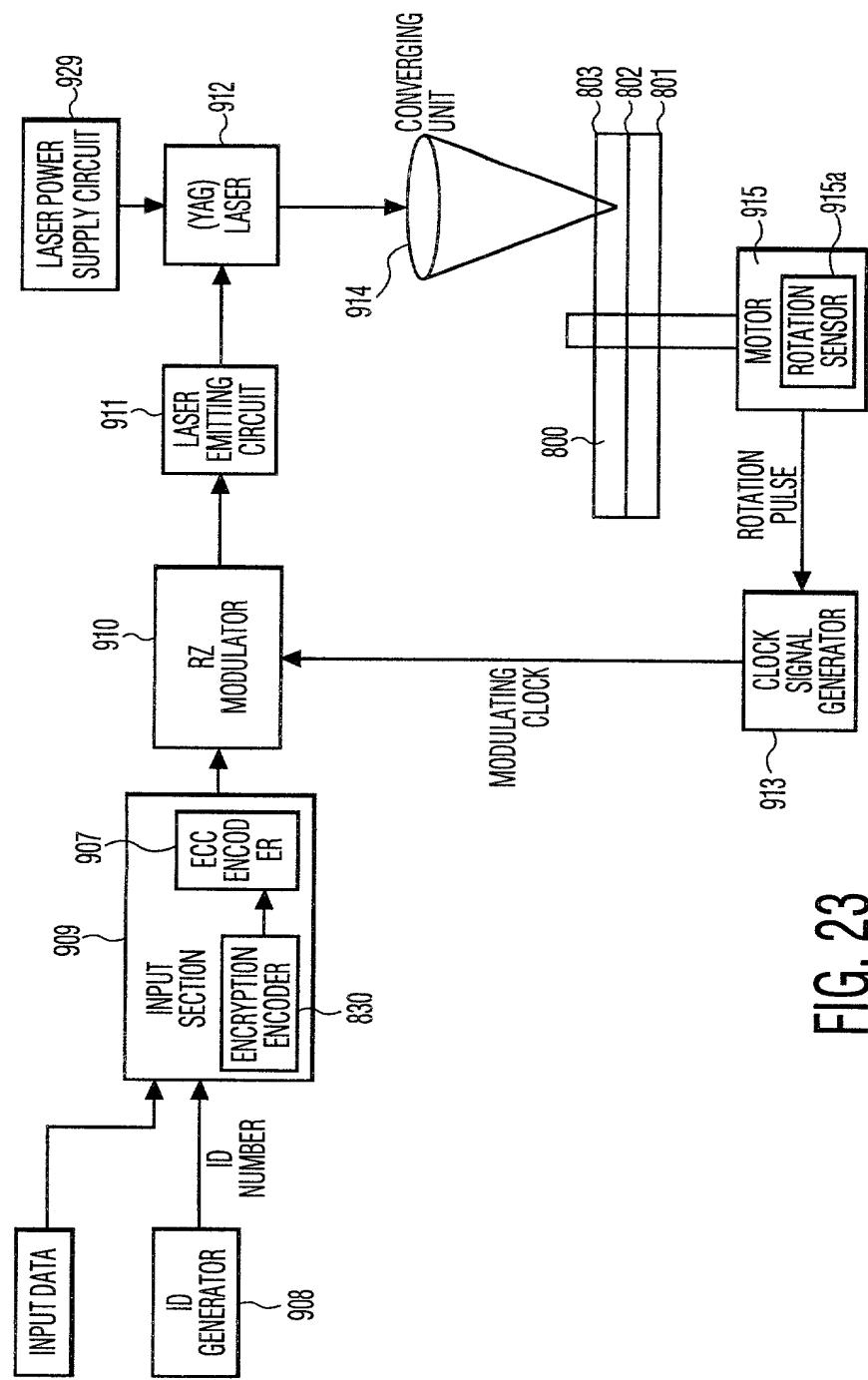


FIG. 23

RZ RECORDING  
MODULATION CLOCK  
BASED ON ROTATION  
PULSE

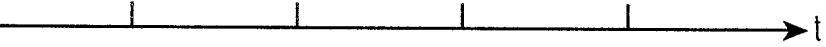


FIG. 24A (1) RECORDED SIGNAL OF "00"

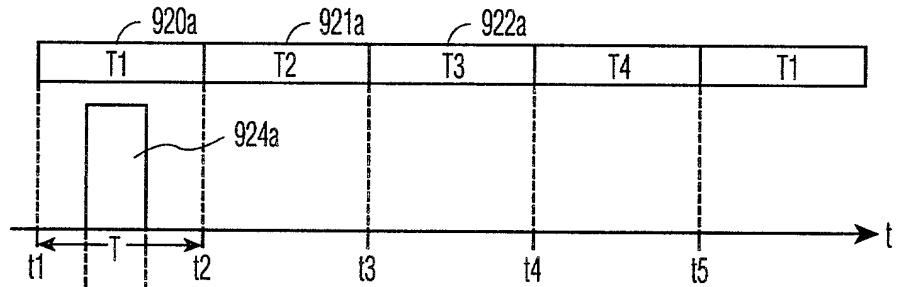


FIG. 24B

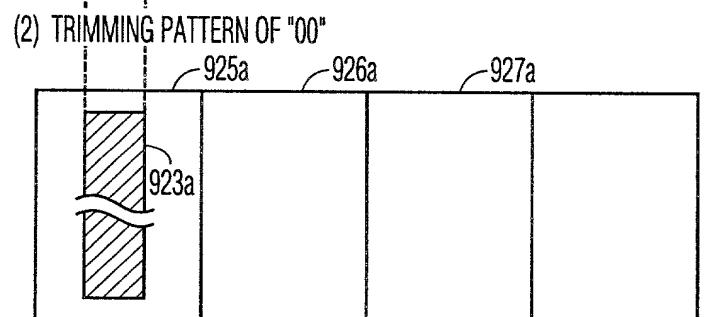


FIG. 24C

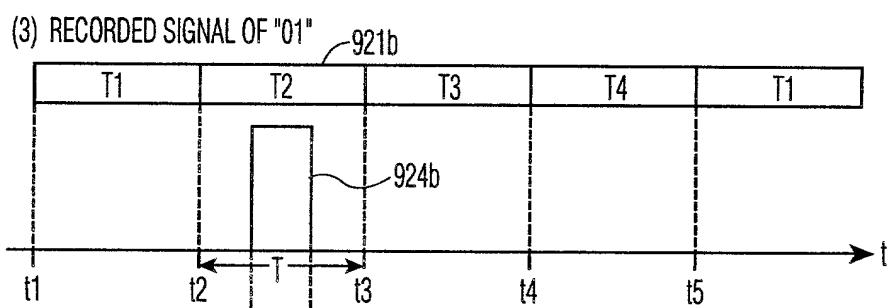


FIG. 24D

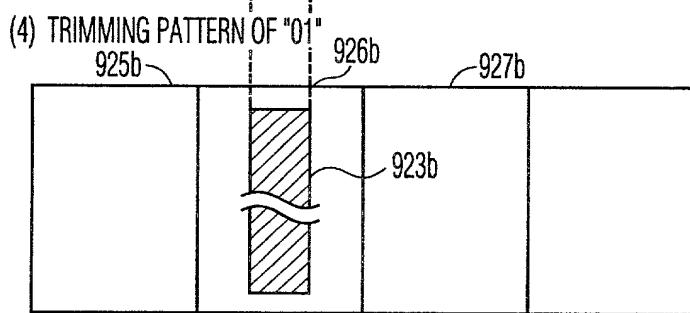


FIG. 24E

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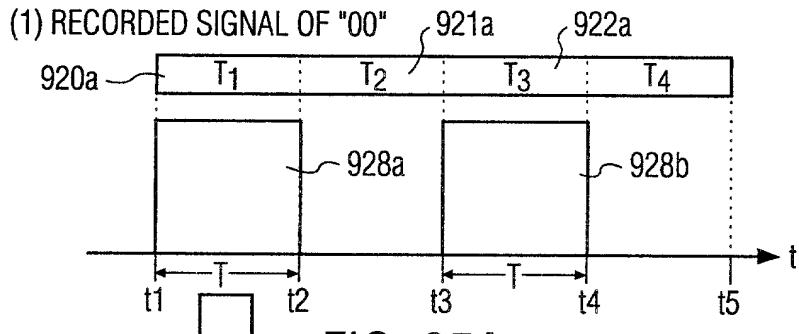


FIG. 25A

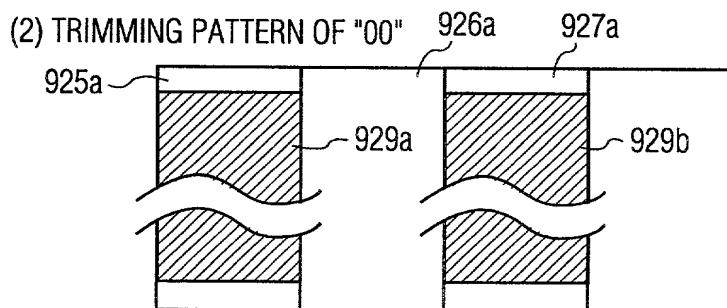


FIG. 25B

(3) RECORDING SIGNAL OF "10"

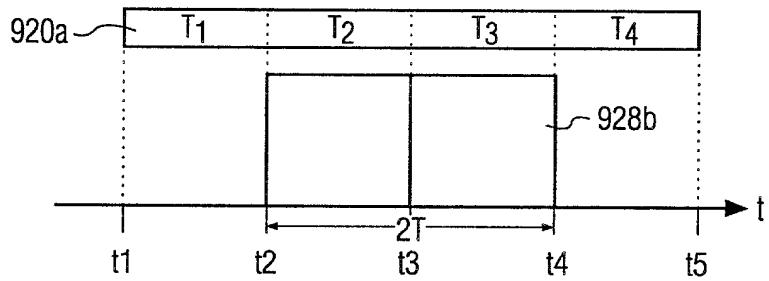


FIG. 25C

(4) TRIMMING PATTERN OF "10"

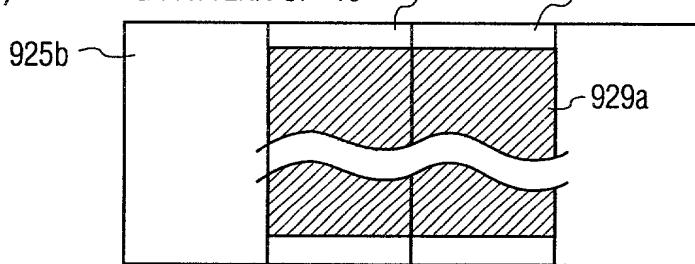


FIG. 25D

## PE-RZ RECORDING

RECORDING  
CLOCK

(1) RECORDED SIGNAL OF "0"

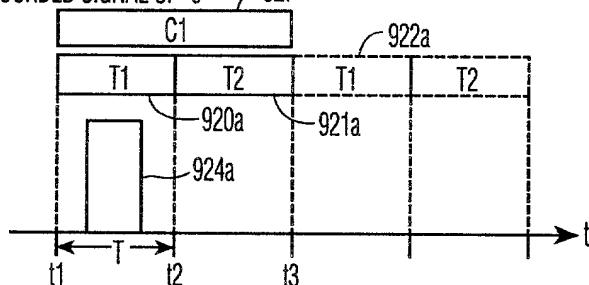


FIG. 26A

(2) TRIMMING PATTERN OF "0"

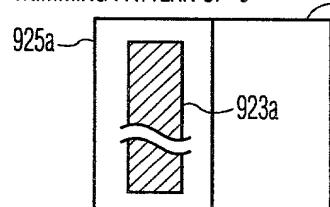


FIG. 26B

(3) RECORDED SIGNAL OF "1"

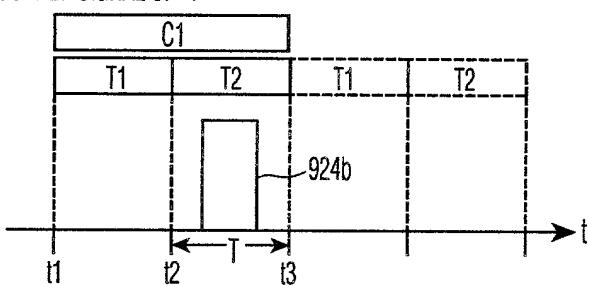


FIG. 26C

(4) TRIMMING PATTERN OF "1"

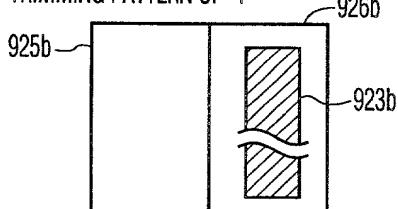


FIG. 26D

(4) RECORDED SIGNAL OF "010"

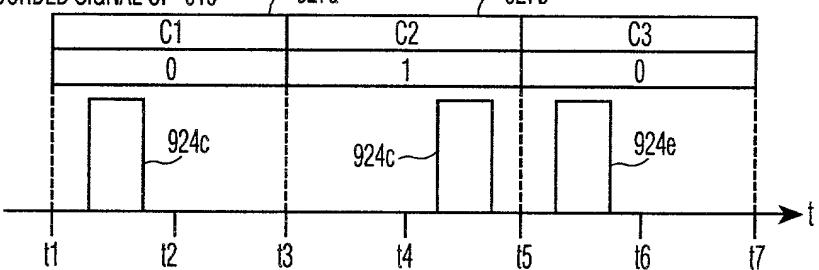


FIG. 26E

(1) TOP PLAN VIEW

FIG. 27A

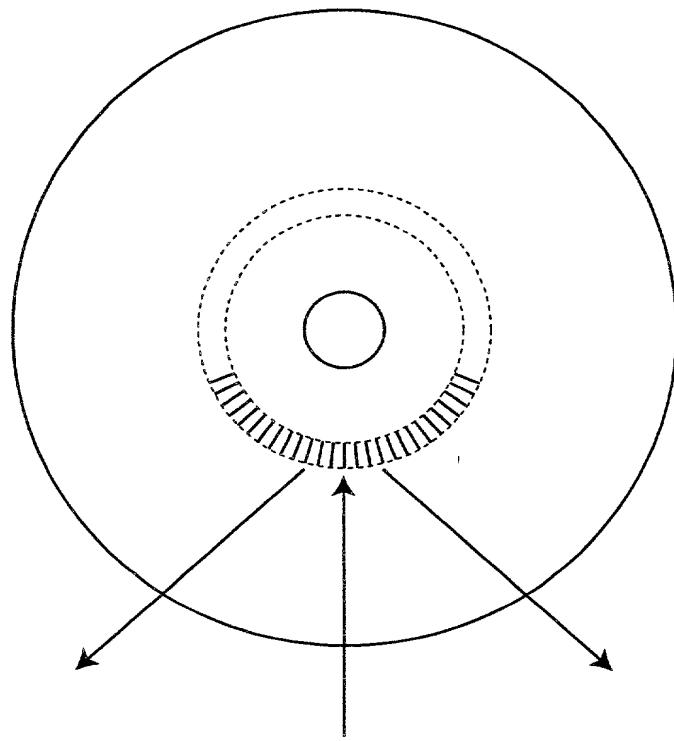


FIG. 27B

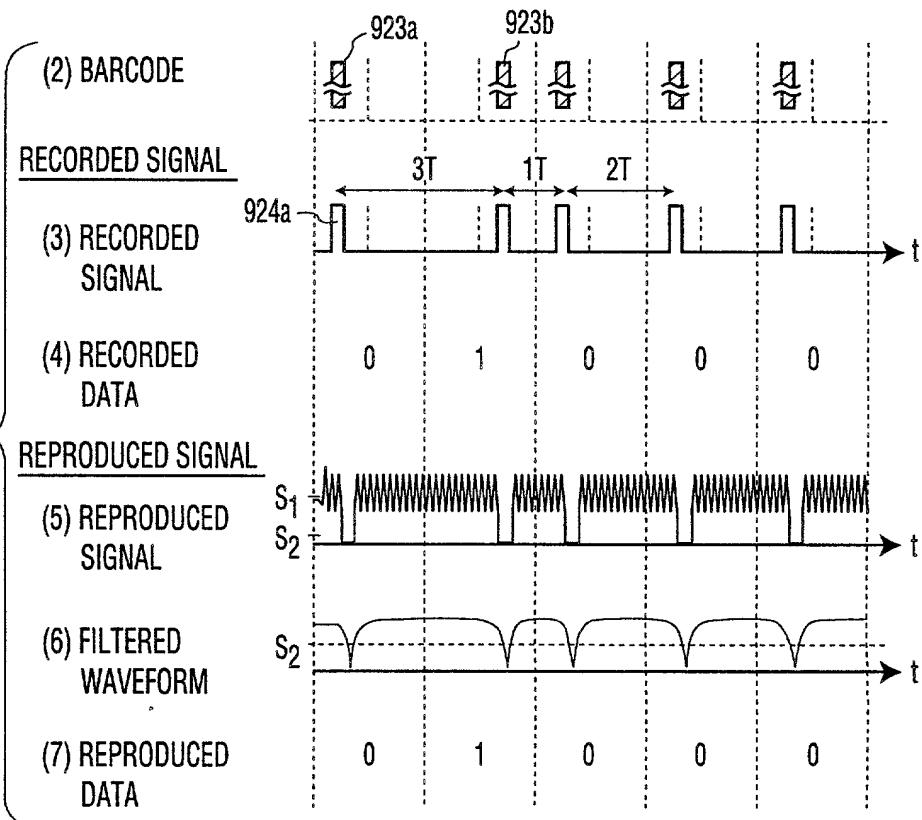


FIG. 28A

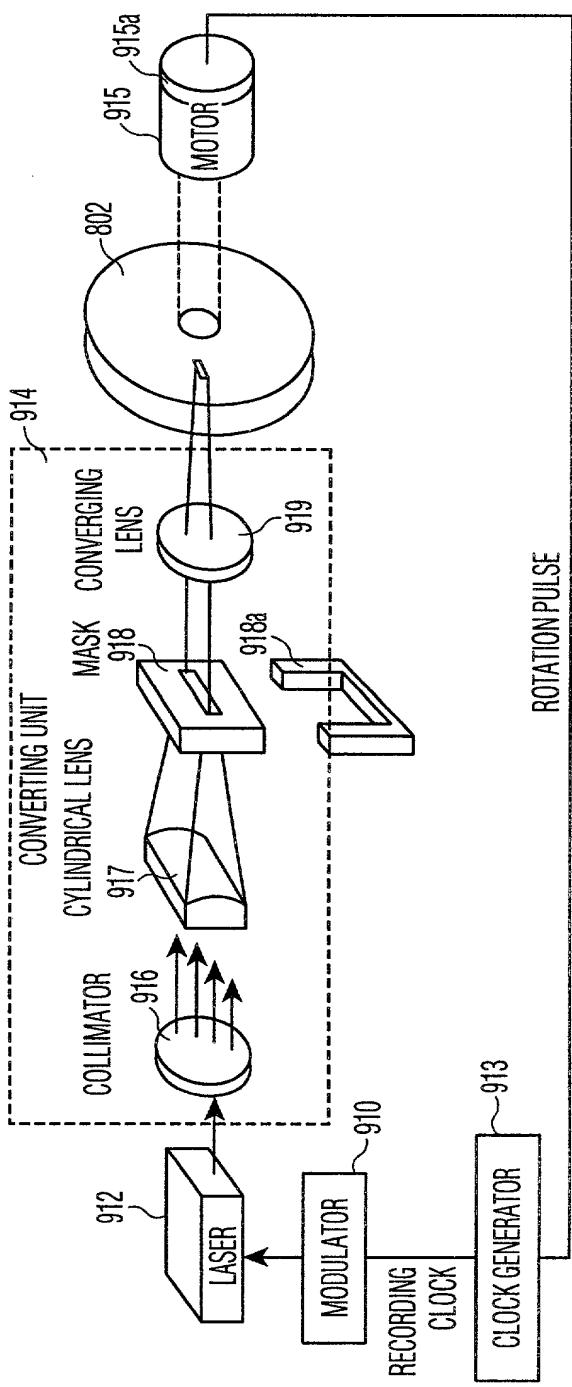


FIG. 28B

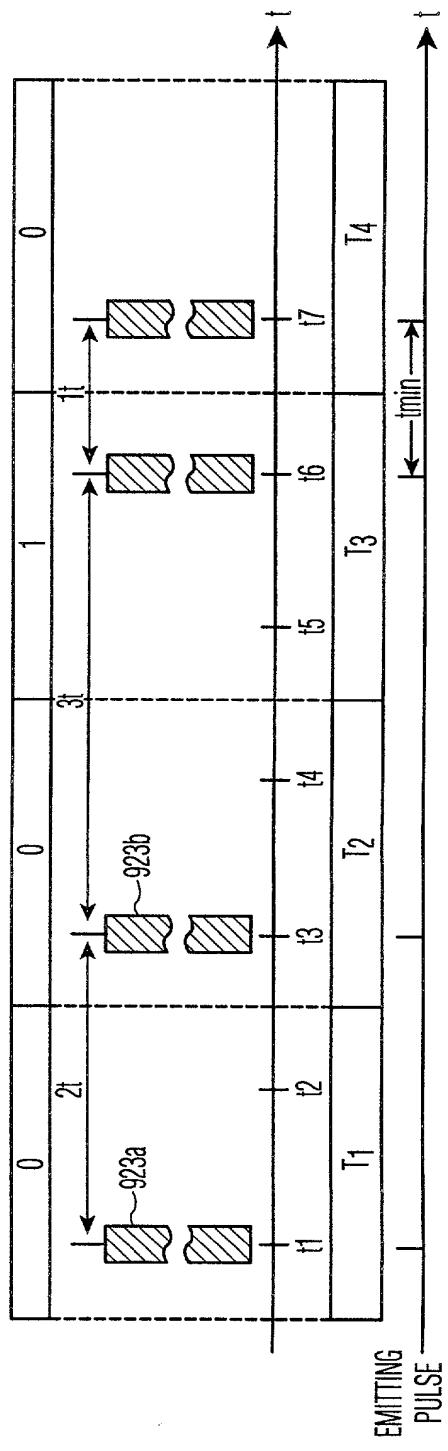


FIG. 29A

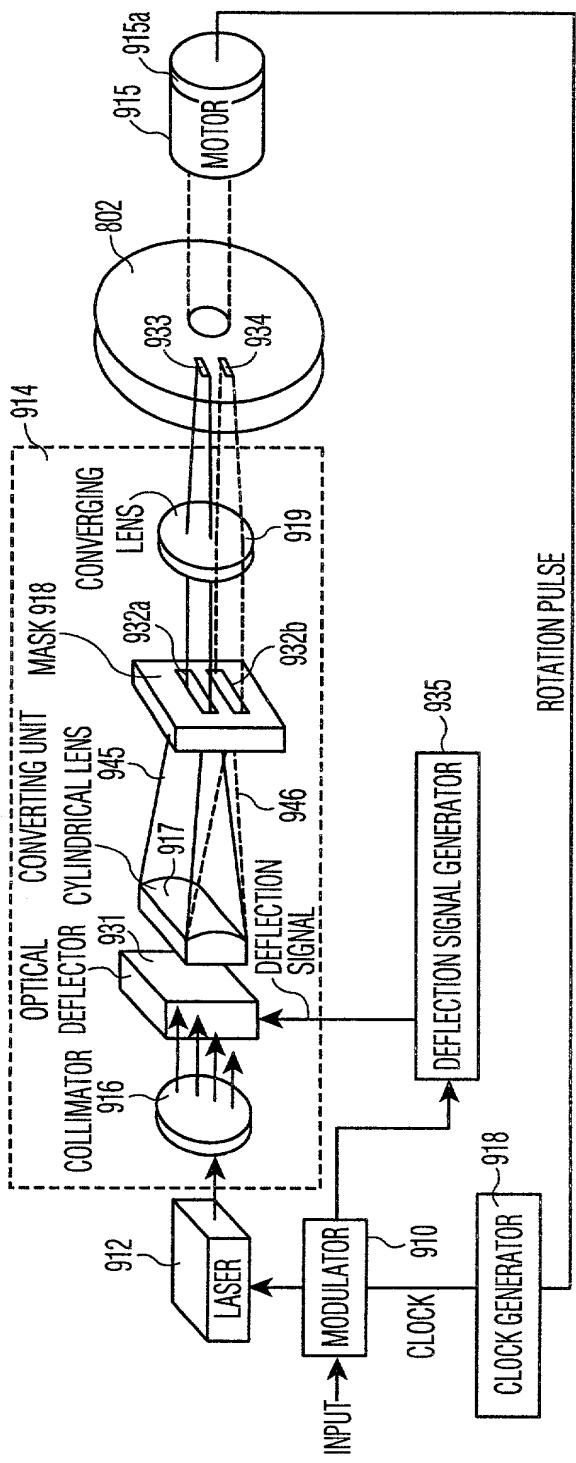
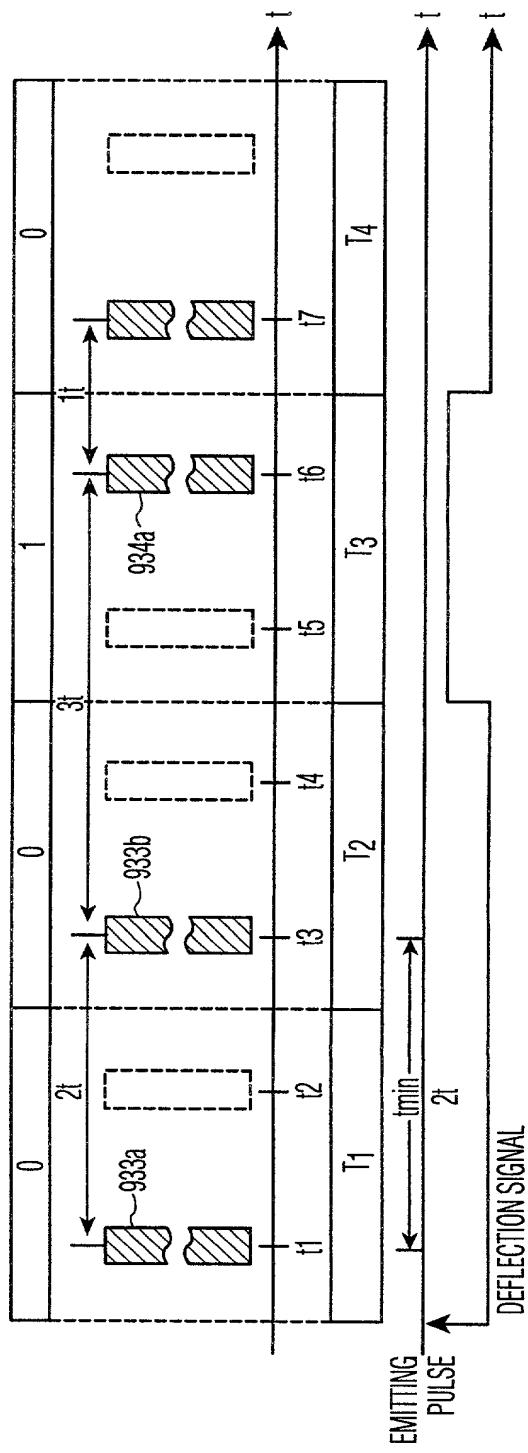
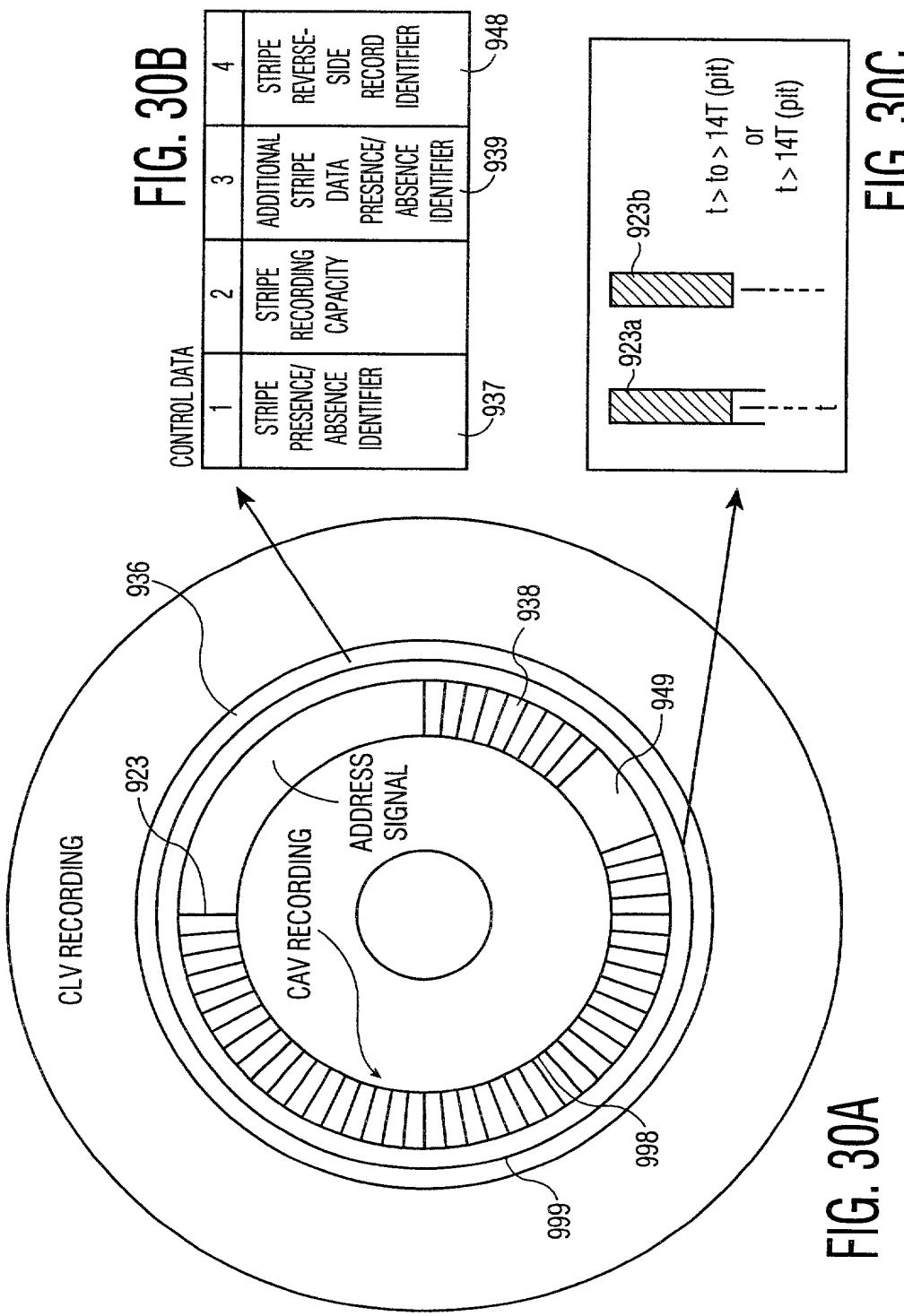


FIG. 29B





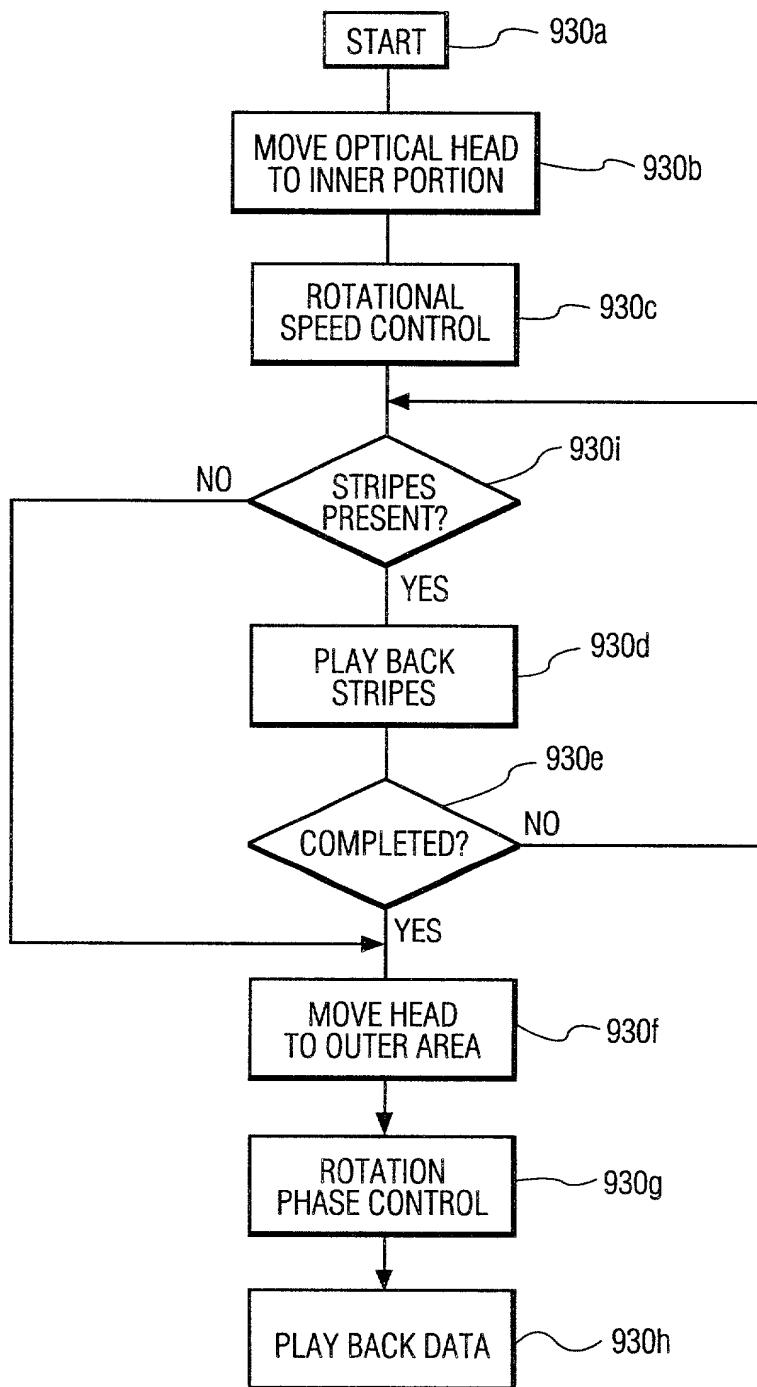


FIG. 31

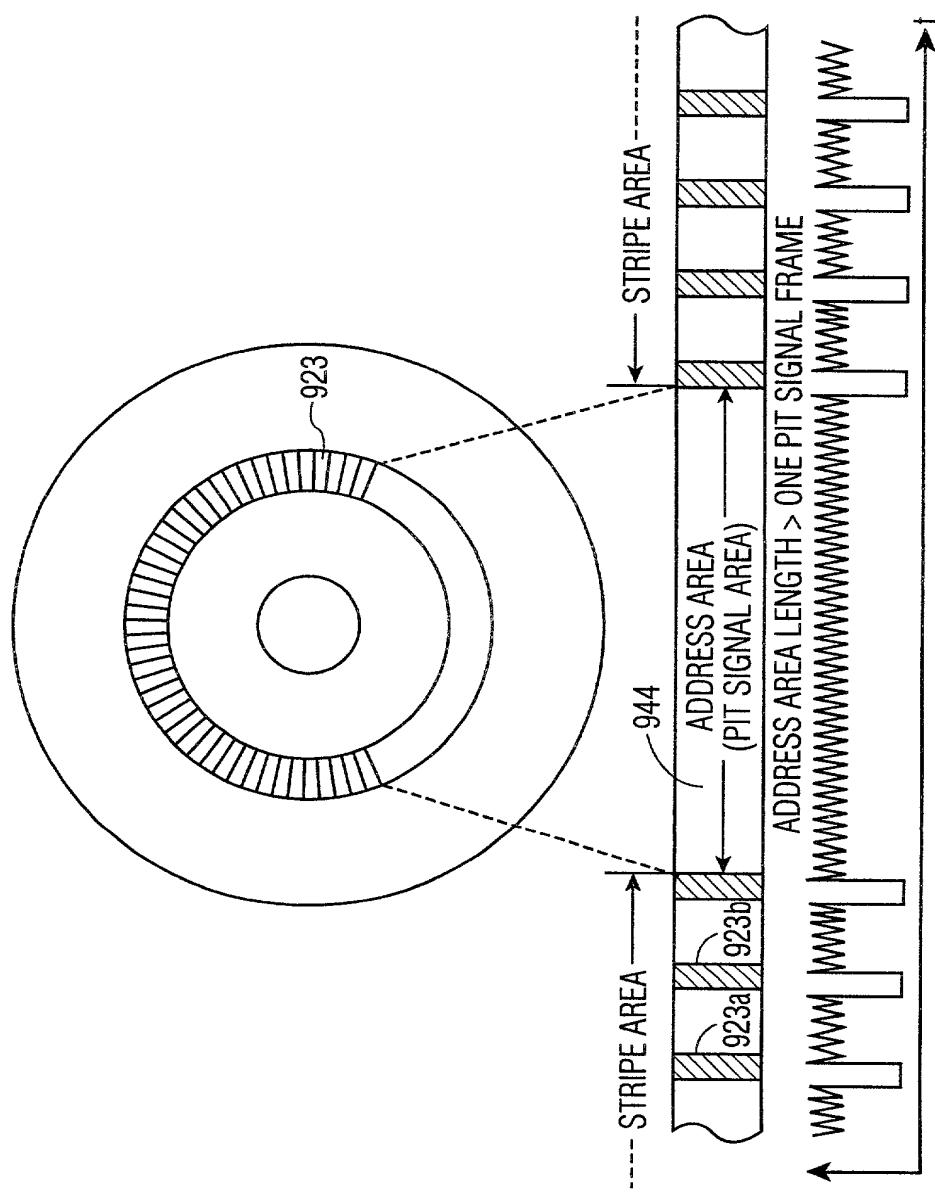


FIG. 32

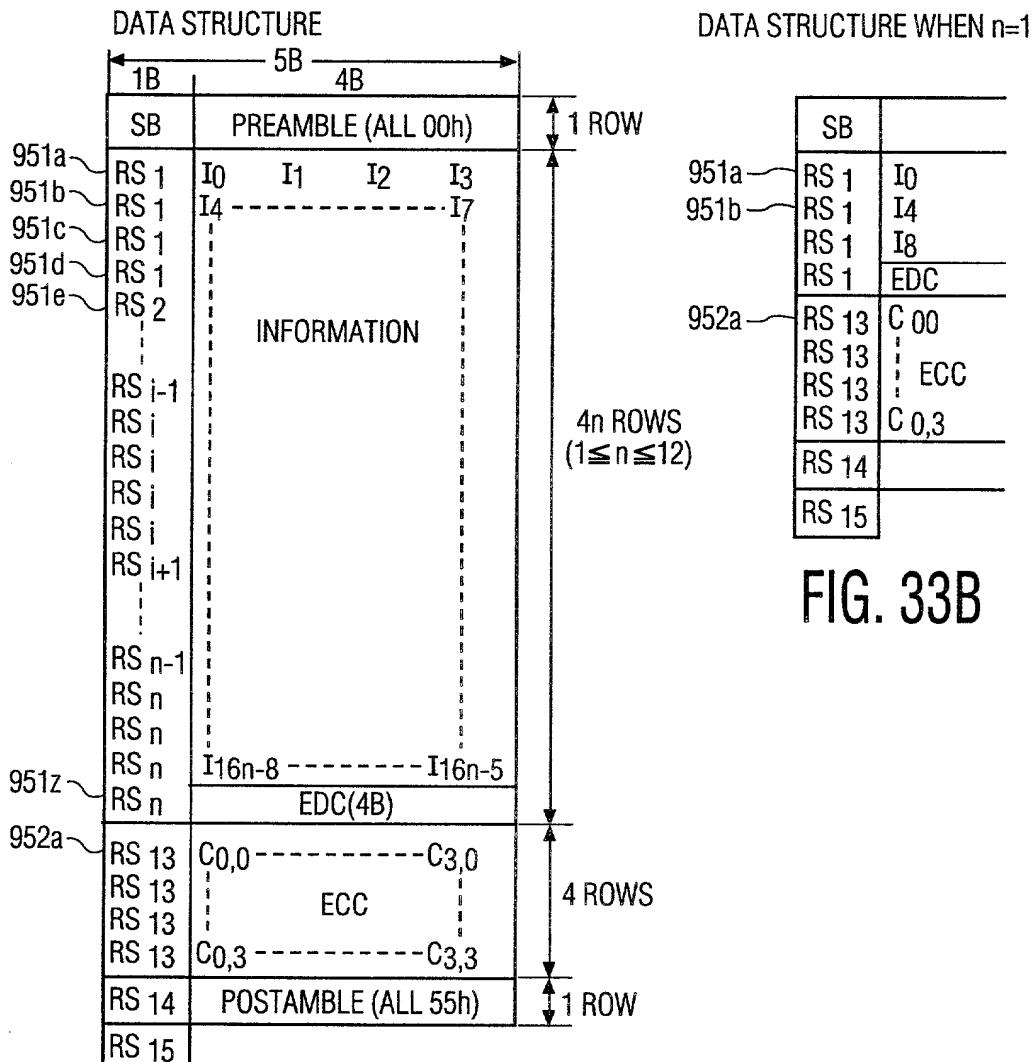


FIG. 33A

RANDOM ERROR CORRECTION CAPABILITY	
BIT ERROR RATE BEFORE CORRECTION	READ ERROR RATE AFTER CORRECTION
$10^{-5}$	1 IN $10^{10}$ DISKS
$10^{-4}$	1 IN $10^7$ DISKS
$10^{-3}$	1 IN $10^4$ DISKS

BURST ERROR CORRECTION CAPABILITY	

FIG. 33C

## SYNCHRONIZATION CODE DATA

## SYNCHRONIZATION CODE

SYNC BYTE /RESYNC	BIT PATTERN											
	FIXED PATTERN (CHANNEL BIT)							SYNC CODE (DATA BIT)				
	C <sub>15</sub>	C <sub>14</sub>	C <sub>13</sub>	C <sub>12</sub>	C <sub>11</sub>	C <sub>10</sub>	C <sub>9</sub>	C <sub>8</sub>	b <sub>3</sub>	b <sub>2</sub>	b <sub>1</sub>	b <sub>0</sub>
SB	0	1	0	0	0	1	1	0	0	0	0	0
RS <sub>1</sub>	0	1	0	0	0	1	1	0	0	0	0	1
RS <sub>2</sub>	0	1	0	0	0	1	1	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
RS <sub>1</sub>	0	1	0	0	0	1	1	0	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
RS <sub>15</sub>	0	1	0	0	0	1	1	0	1	1	1	1

FIG. 34A

## FIXED SYNCHRONIZATION PATTERN

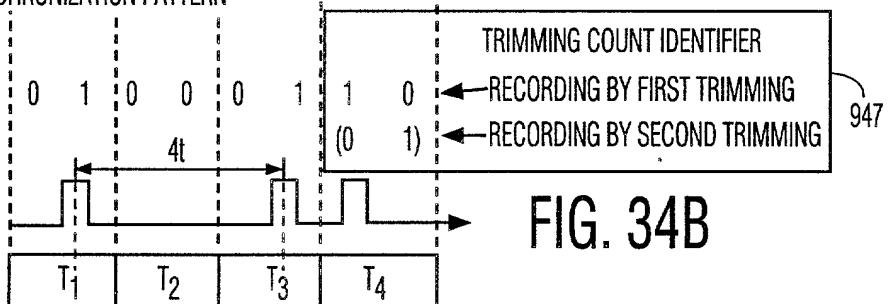


FIG. 34B

## MAXIMUM CAPACITY

	RECORDING CAPACITY	TOTAL BYTE COUNT	EFFICIENCY	RECORDING AREA ANGLE	UNRECORDED AREA ANGLE
MINIMUM	12B	41B	29.3%	51 DEGREES	309 DEGREES
MAXIMUM	188B	271B	69.4%	336 DEGREES	24 DEGREES

FIG. 34C

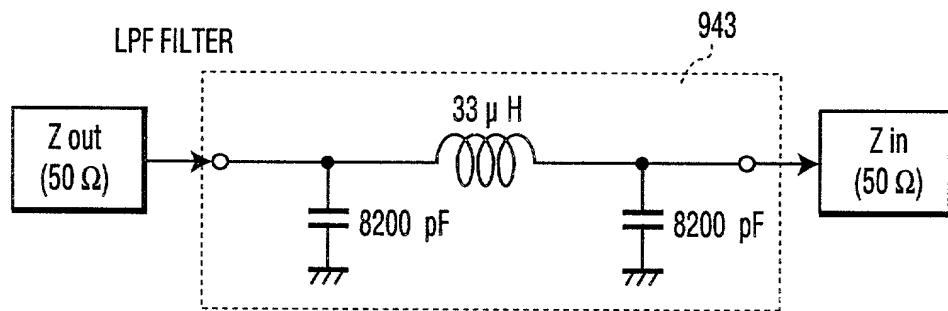


FIG. 35A

SIMULATOR WAVEFORM AFTER LPF :  $I_{14L} = I_S = 0.1$ 

FIG. 35B

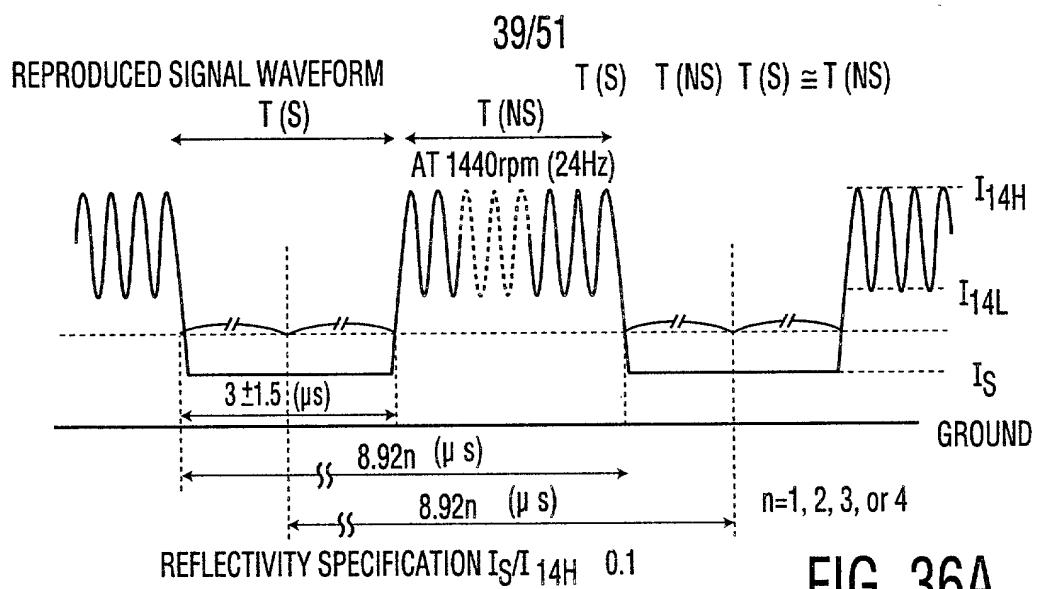


FIG. 36A

DIMENSIONAL ACCURACY OF SLIT (AT  $r=22.2\text{mm}$ )

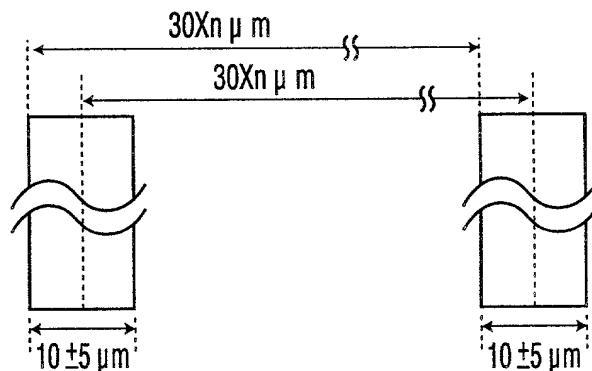


FIG. 36B

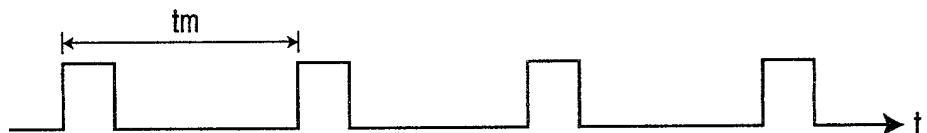


FIG. 36C

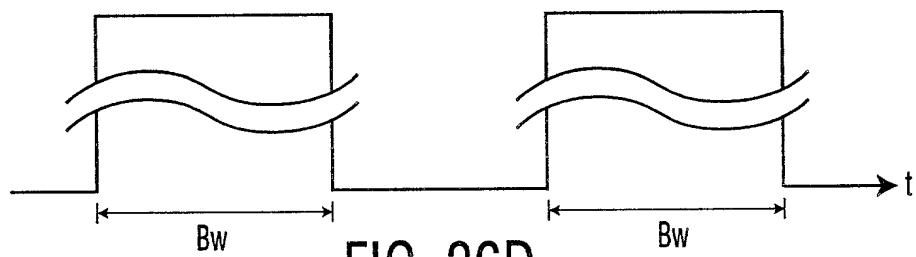


FIG. 36D

(1) TIME SLOT

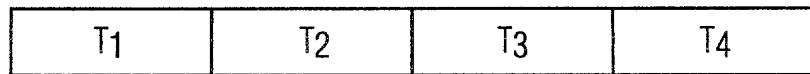


FIG. 37A

(2) CHANNEL BIT

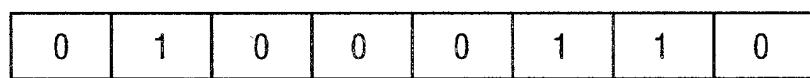


FIG. 37B

(3) RECORDING PULSE

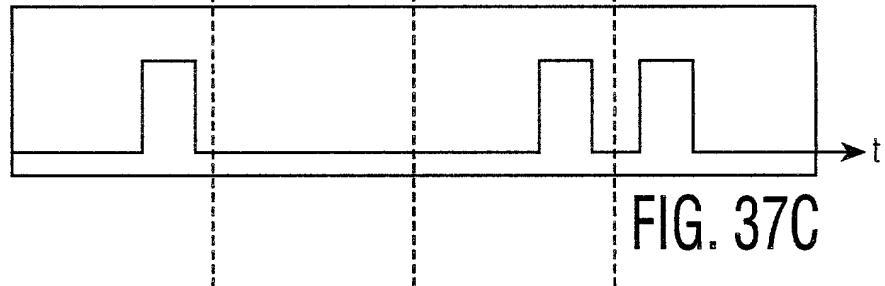


FIG. 37C

(4) EMITTING PULSE

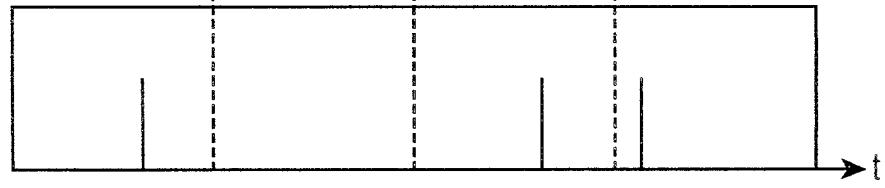


FIG. 37D

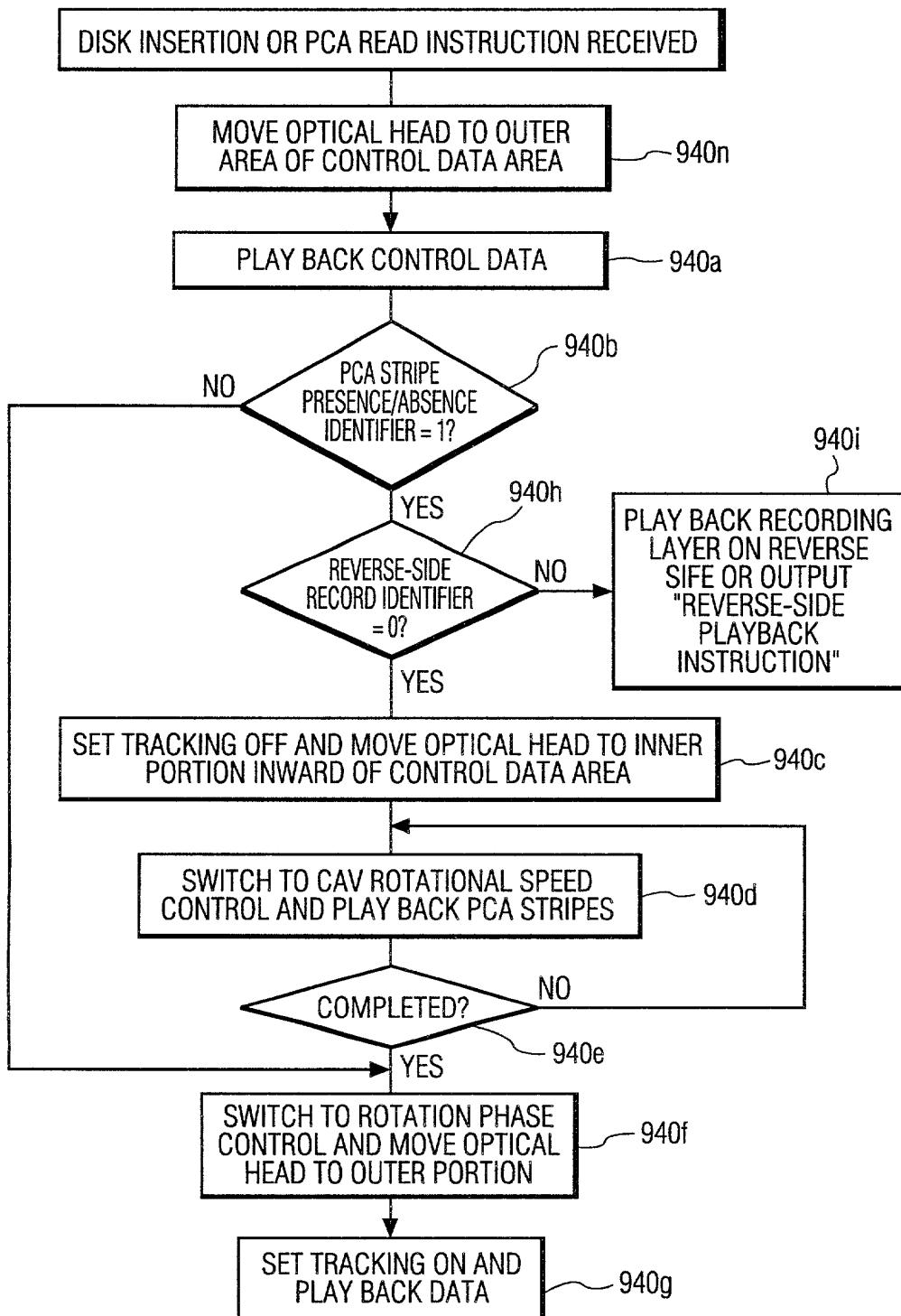
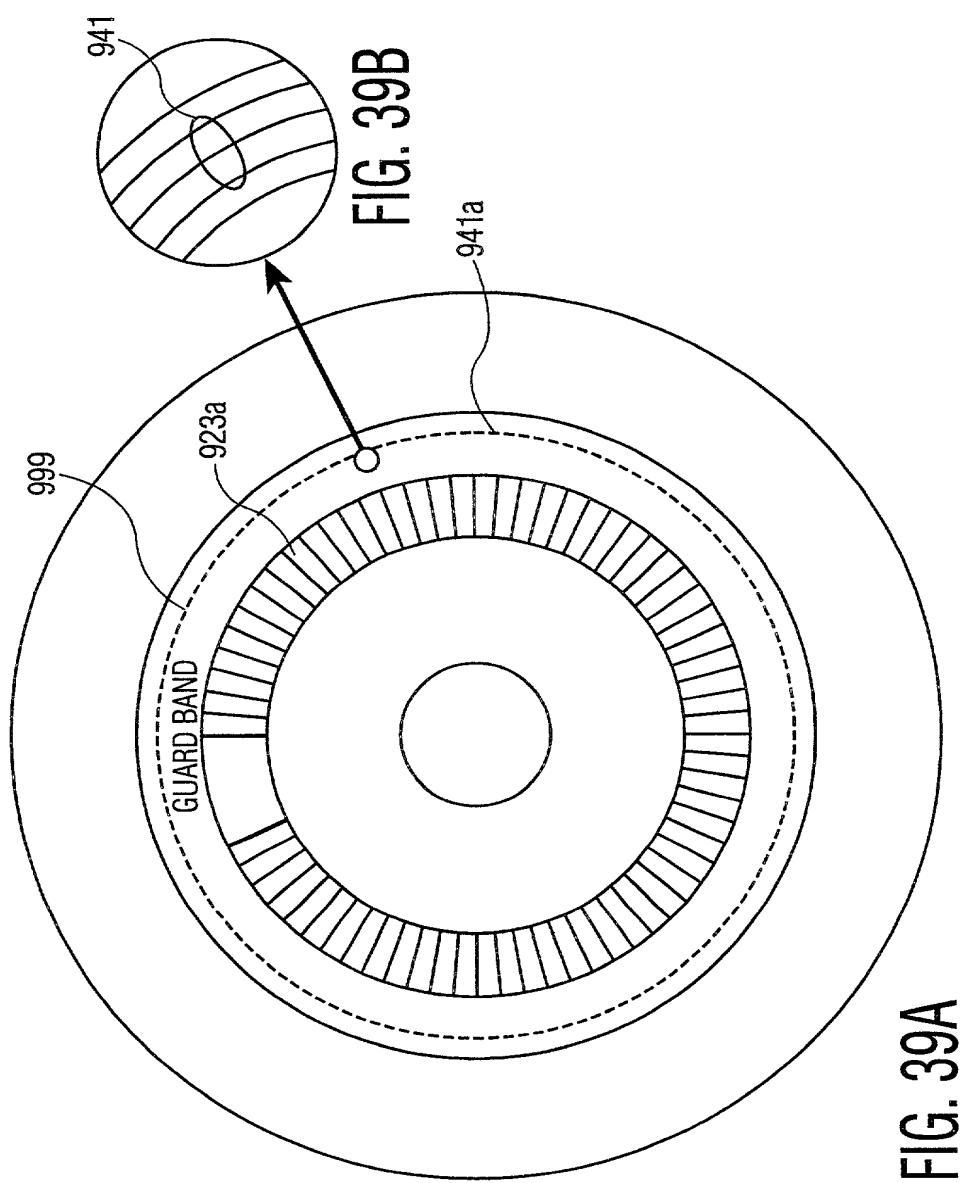


FIG. 38



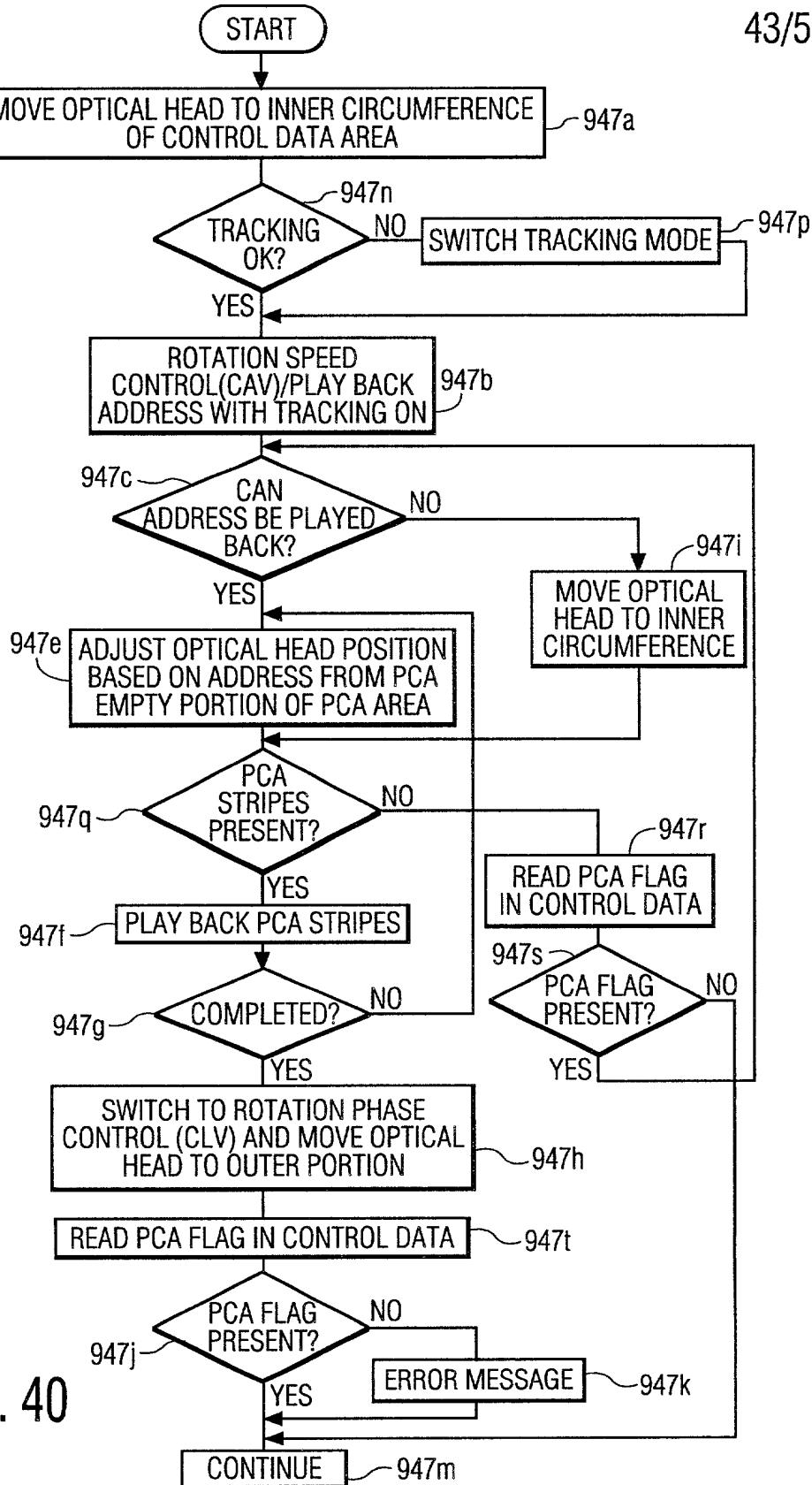


FIG. 40

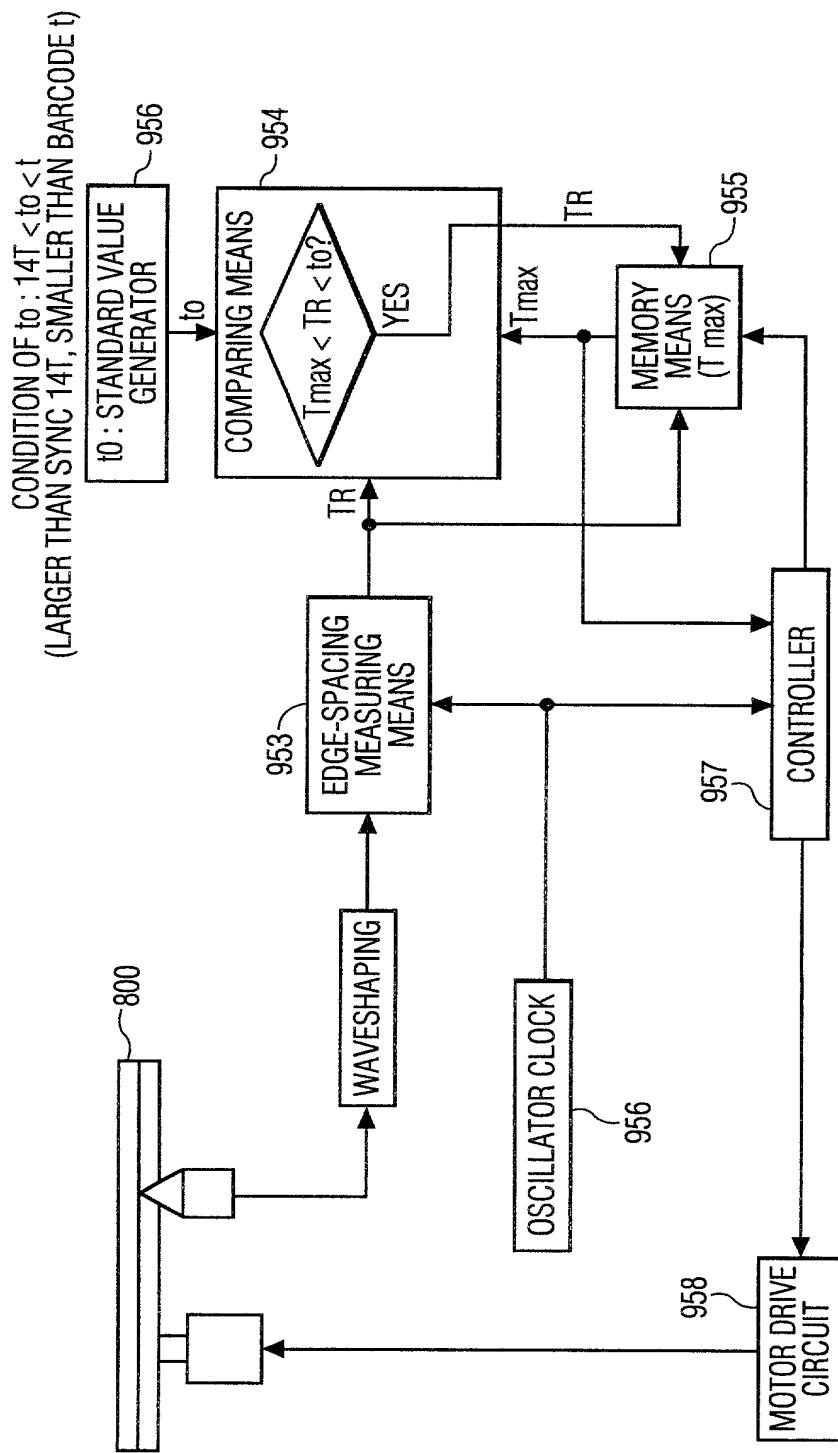


FIG. 41

800 953 956 957 958 959 954a 955a

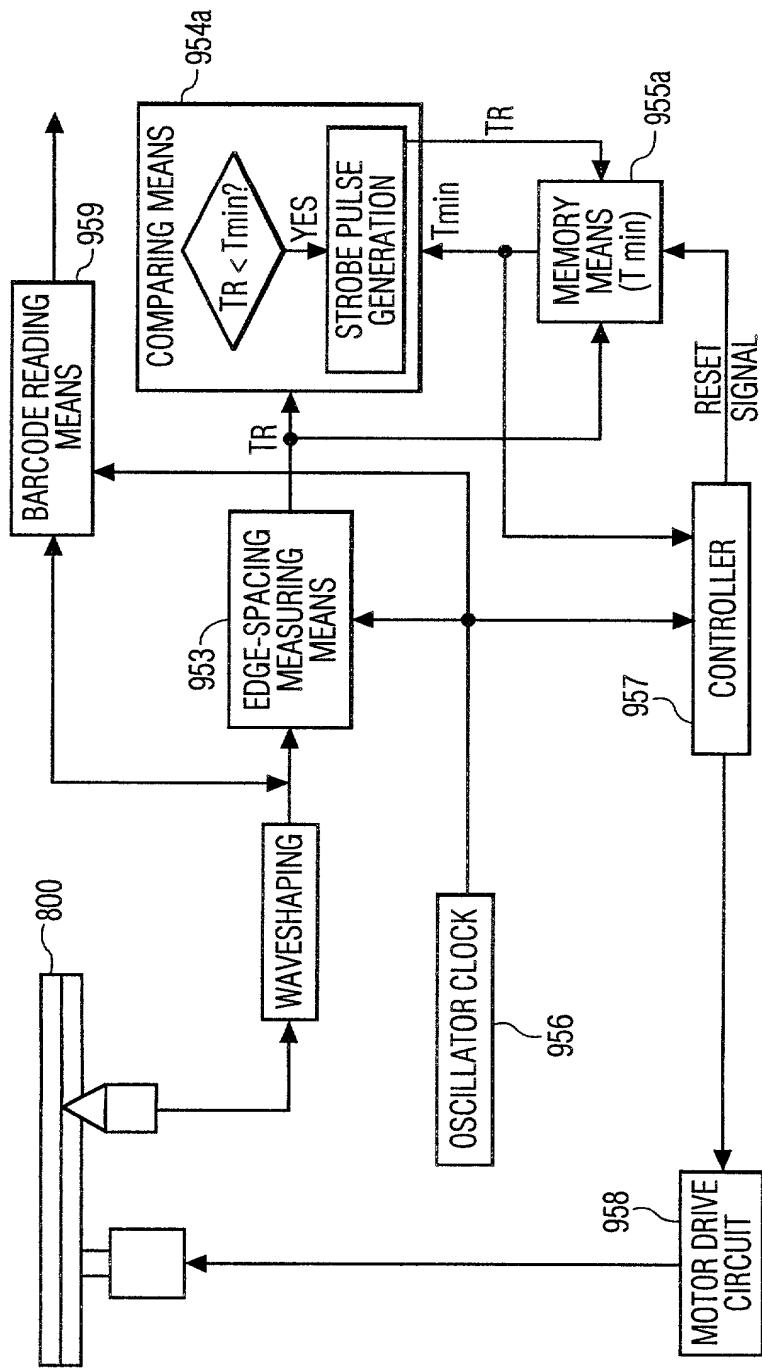


FIG. 42

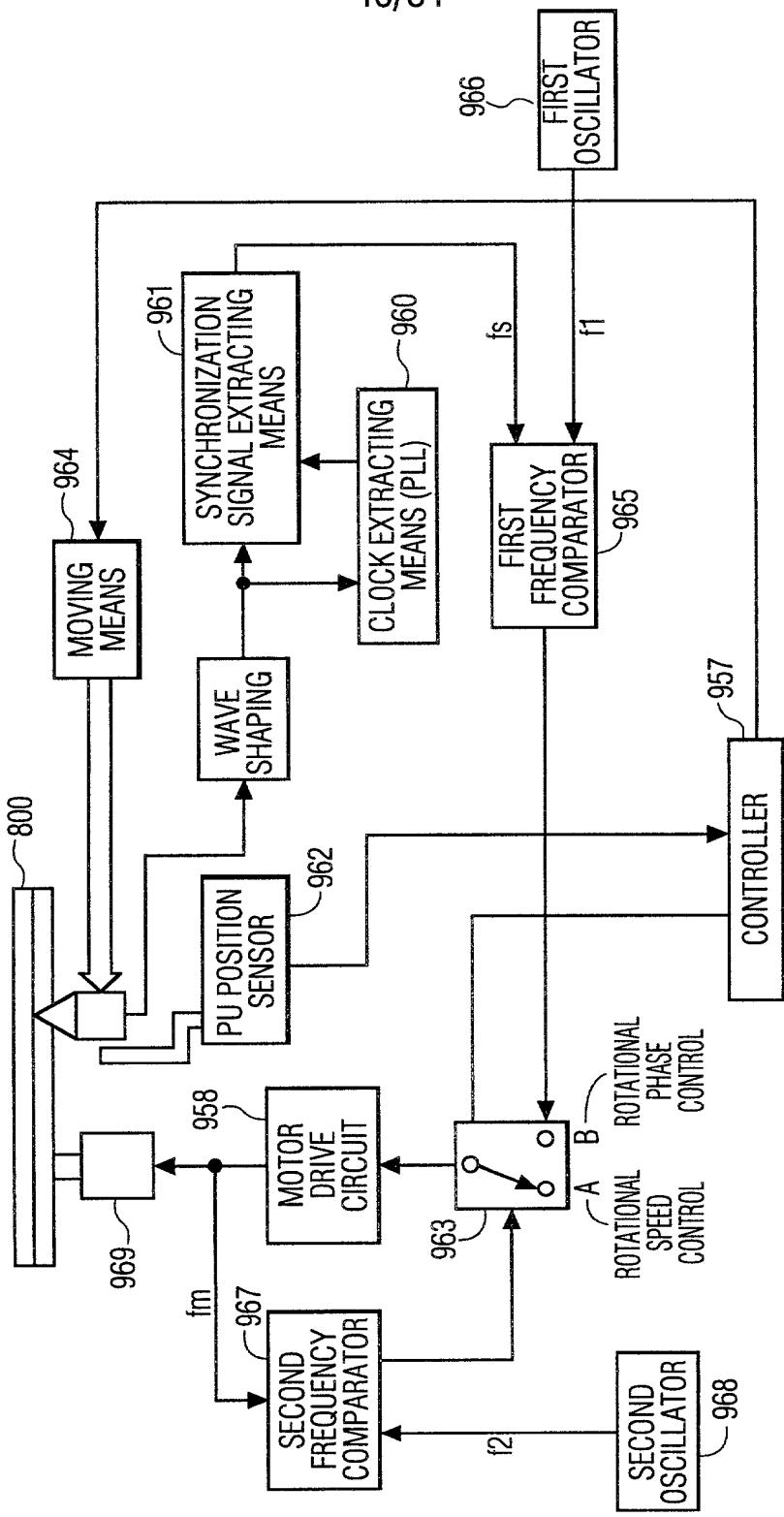


FIG. 43

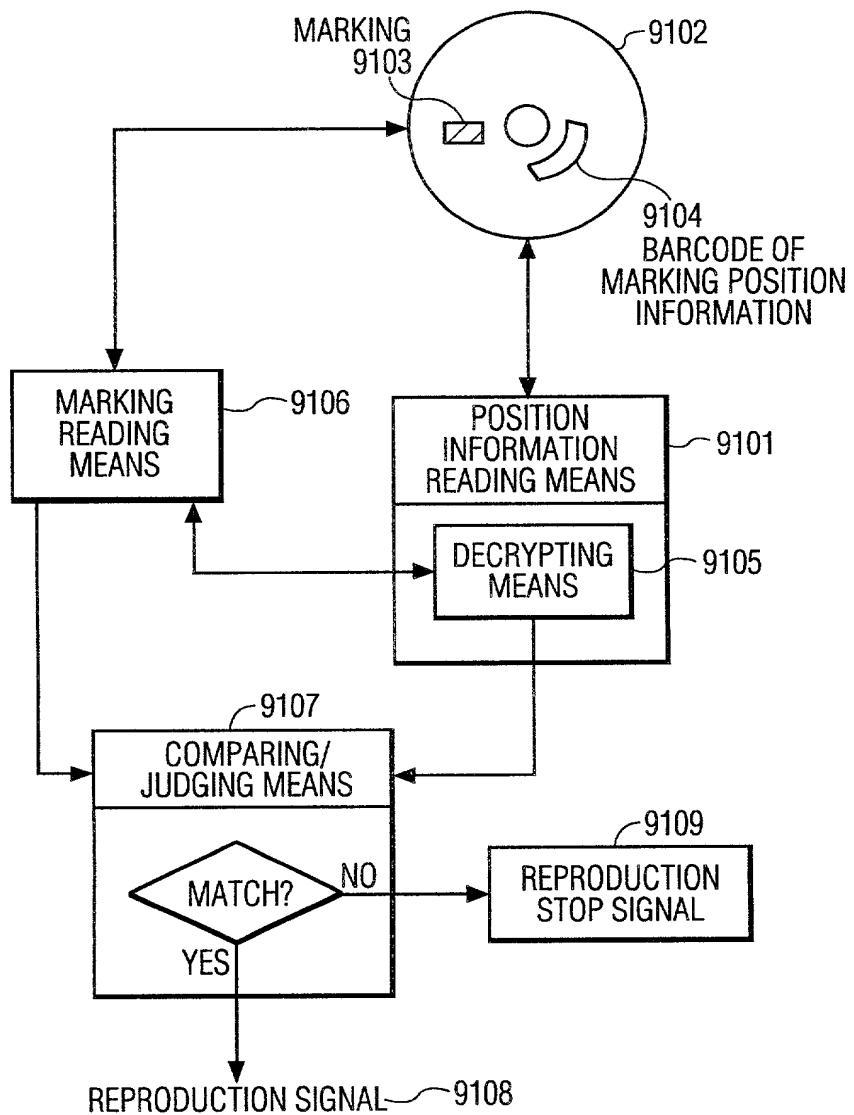
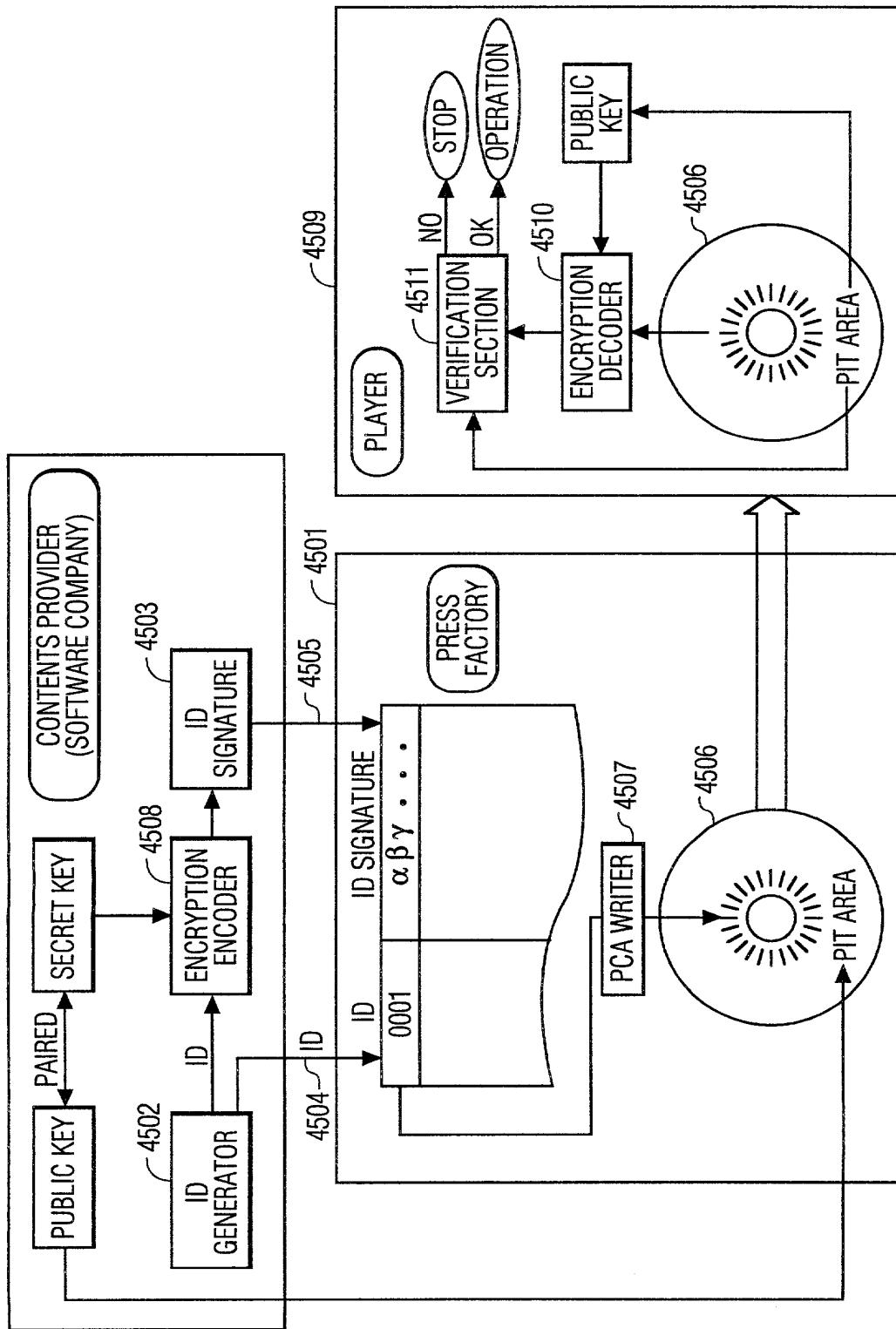
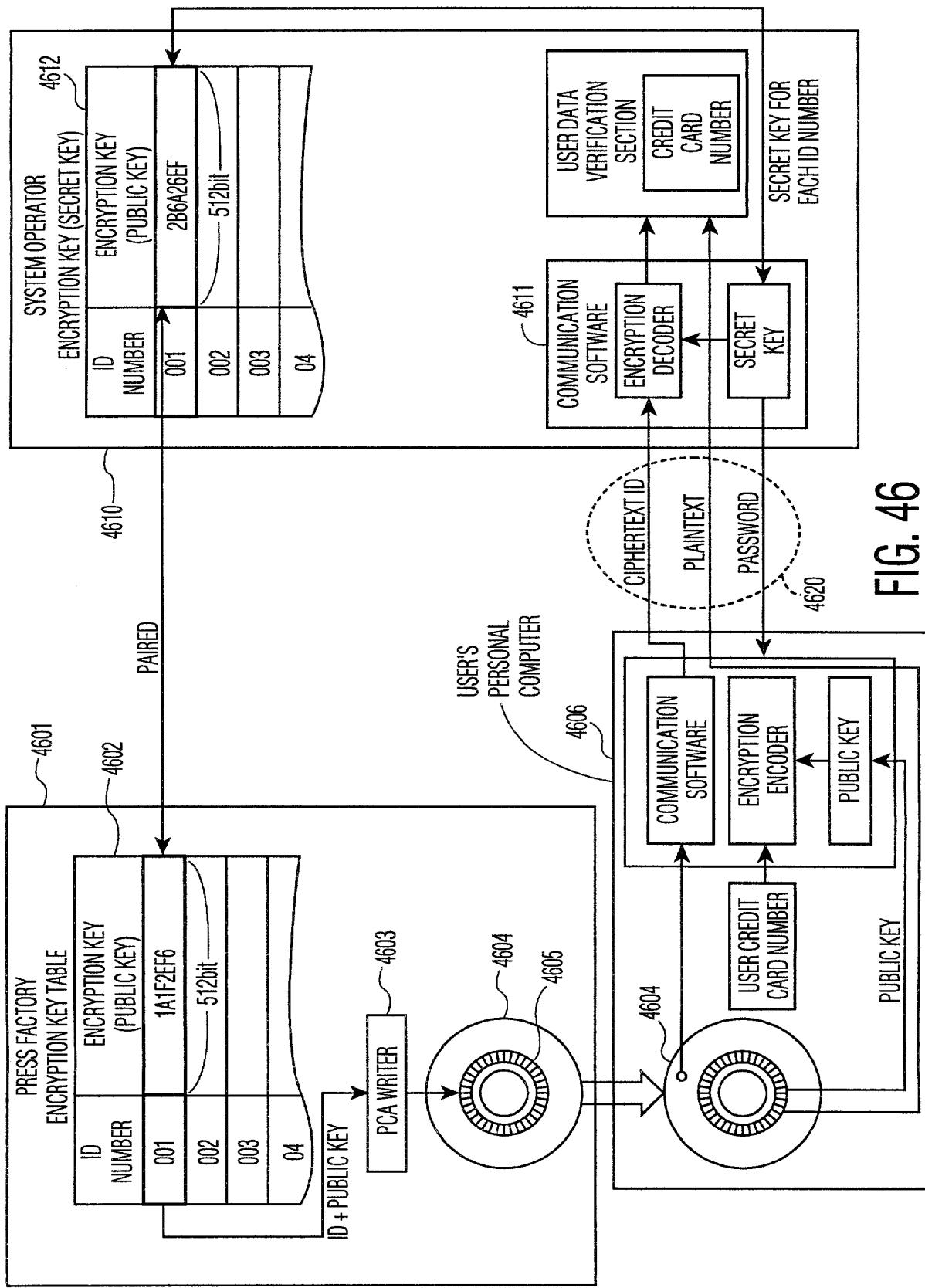


FIG. 44

FIG. 45





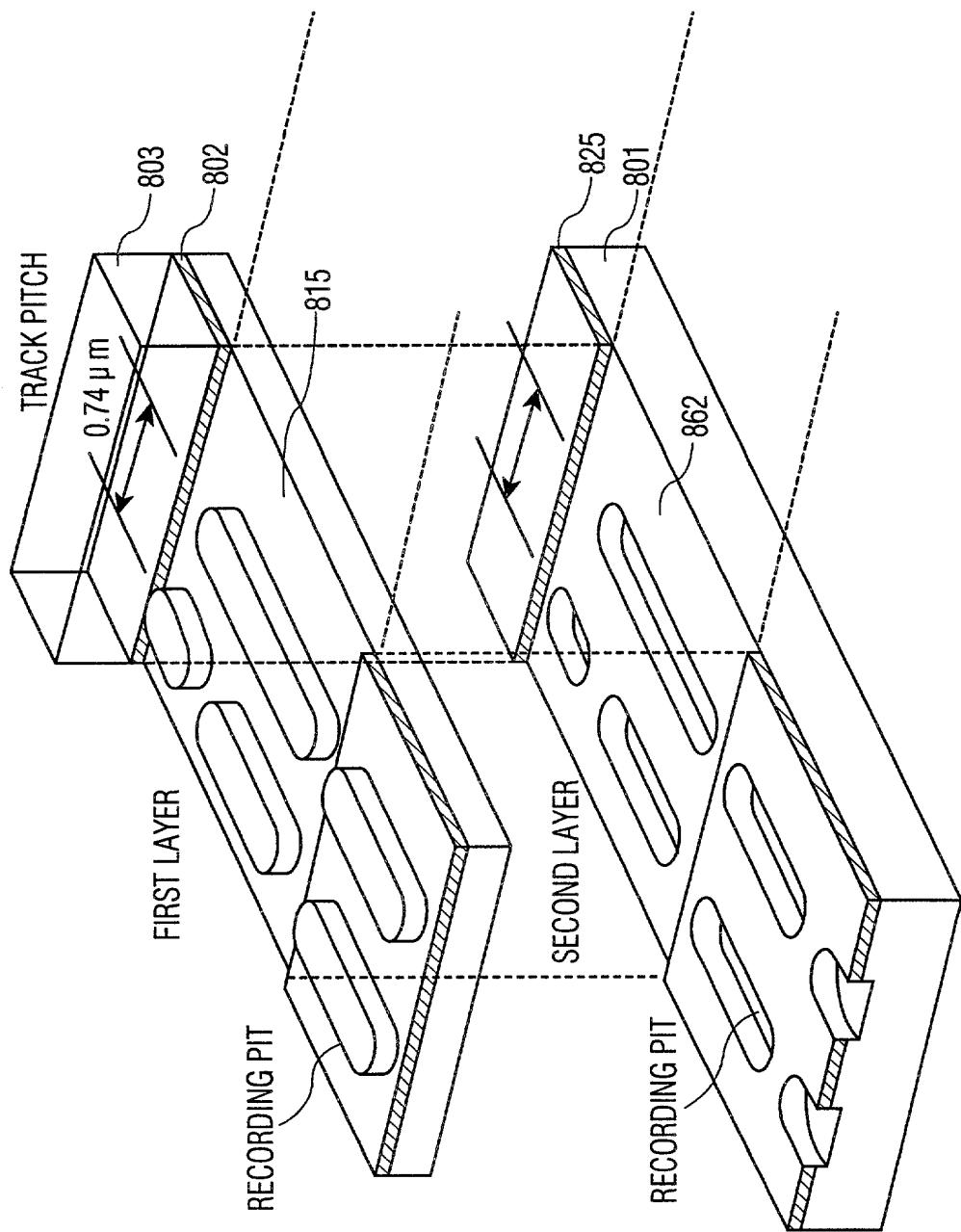


FIG. 47

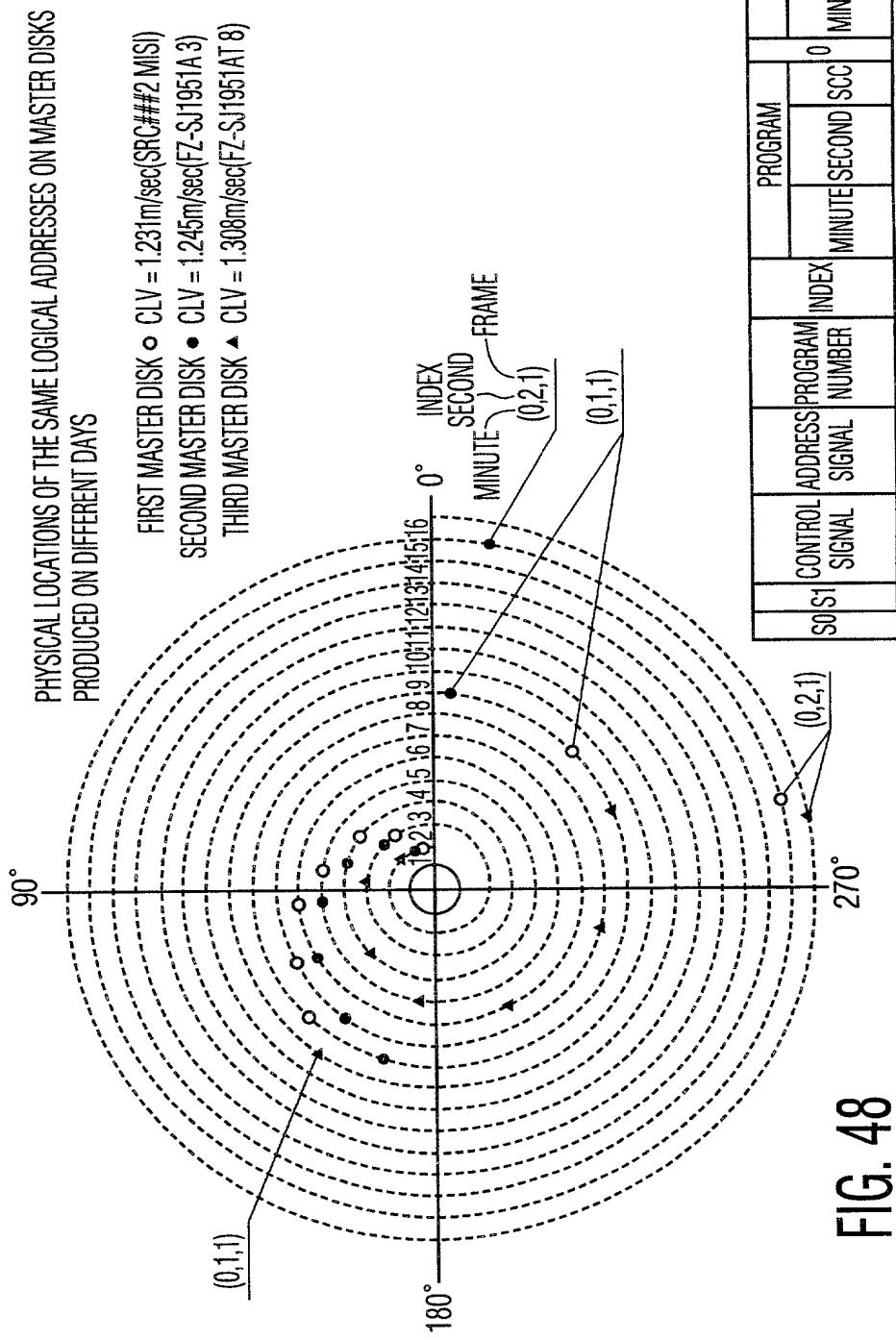


FIG. 48